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⑥ DATA STORAGE METHOD AND APPARATUS

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DATA STORAGE METHOD AND APPARATUS

2 This invention relates to random access data storage
3 systems, and more particularly, to random access data recording
4 systems for selectively writing, reading or erasing such data wherein
5 direct access can be obtained to individual strings of data, e.g., tracks
6 of magnetically recorded data.

In general, prior art data storage systems rely upon the programmer to select an address for a particular unit of data to write the data into storage, to determine whether the data will overflow the space allotted for a particular record, to determine and select the address or addresses for the overflow portion of the data to be written, to address the random access mechanism to find and read a desired record and to find and read the corresponding overflow data, and to address the random access mechanism to find and erase a selected record and to find and erase the corresponding overflow data. To accomplish this, the address associated with each data record is highly complex, including characters representative of (1) the disk or drum upon which a data record is written, (2) the particular track upon which the record is written, (3) the particular sector of the track upon which the record is written, and (4) the particular record itself.

21 Thus, the effort required of the programmer to write, read,
22 keep track of, or erase records of data is highly complex and demanding.

23 The job is made even more complex if a record is erased
24 from a first location, perhaps modified, and written in a new location.
25 This is caused by the fact that an address merely describes the location
26 of a record and bears no other relationship to the data. Thus, the
27 address for the record must be completely redefined and all references
28 to that record by its address correspondingly changed.

29 In the usual case, the physical length of the data to be
30 stored is not the same in each instance. The above-described complexity

1 involved in record overflow causes most programmers to establish
2 standard record lengths no smaller than the average or medium data
3 length and more often larger than the average or medium data length.
4 Thus, a considerable portion of the available storage space is wasted
5 because less data is recorded than allowed for by the record length.

6 Some systems attempt to compensate for the variances in
7 data length by utilizing a portion of the memory to establish a format
8 for the remainder of the memory wherein various record lengths are
9 established for each track. Thus, in writing the data the programmer
10 addresses the smallest available record long enough to hold the entire
11 length of data to be written. Of course, if the record of the desired
12 size is occupied, the next larger record would be addressed. Again,
13 if that record is occupied, a larger record must be addressed, and so
14 on, until an empty record is located. Although this system is some-
15 what more space efficient than the system having standard record
16 lengths, a great deal of area therefore still remains wasted including
17 that area used to establish the format.

18 Additionally, the data remains scattered along the track
19 in accordance with the size of each data length thereby requiring an
20 average of one-half a cycle of the memory to begin reading the
21 addressed record and nearly a complete cycle of the memory to read
22 all of the addresses and/or data on a track.

23 Independently of programming problems, existing systems
24 tend to use memory time inefficiently; i.e., memory time lost during
25 execution of program steps may require an additional memory. For
26 example, if a record is to be purged, a search has to be made to
27 discover the address of the record to be purged. A second memory
28 cycle is then required to execute the purge.

29 Another system for attempting to compensate for variances
30 in data length is to leave record lengths completely flexible. However,

1 this necessitates setting aside a portion of each record to describe the
2 length of the record and setting aside some storage space to obtain
3 gaps between records. Further, when a data record is purged or
4 erased, the new data record probably will not be of the same length.
5 Thus, either the new data record will have to be inserted at some
6 other point, will not fill the complete vacant space, or will overflow to
7 another address. Therefore, the complexity of operation and pro-
8 gramming is increased and, over a period of time, the packing
9 efficiency will only be slightly greater.

10 Therefore, it is an object of the present invention to
11 provide a method of organizing a cyclical file to eliminate programming
12 complexity in writing or reading desired data.

13 Another object of the present invention is to provide a data
14 storage system which automatically writes data in the first available
15 record area without direction or control by the programmer thereby
16 continually tending to pack data together.

17 Another object of the present invention is to provide a
18 method of storing data in cyclical memories which eliminates the need
19 to associate a complex address with each data record.

20 Still another object of the present invention is to provide a
21 data storage system for automatically writing or reading data without
22 having a complex address written with each data record.

23 Yet another object of the present invention is to provide a
24 method of organizing a cyclical file which conserves available storage
25 space and substantially reduces wasted storage space.

26 A further object of the present invention is to provide a
27 data storage system which automatically organizes the stored data to
28 conserve available storage space and substantially reduce wasted
29 storage space.

30 A still further object of the present invention is to provide

1 a method for purging stored data from a storage means in a single
2 cycle of the memory without actually erasing the data to be purged.

3 Another object of the present invention is to provide a data
4 storage system accomplishing selective purging of stored data in a
5 single cycle of the memory without actually erasing the data to be
6 purged.

7 A further object of the present invention is to provide a
8 method of organising a cyclical file which automatically packs
9 data towards the first unit of stored data on a cyclical unit
10 such as a track.

11 Yet another object of the present invention is to provide a
12 data storage system for automatically packing the data towards the
13 first unit of data in a cyclical unit of the file, such as a track, so as to
14 reduce the time required to read all of the addresses and/or data on
15 the cyclical unit.

16 Therefore, in accordance with the present invention there
17 is provided a method of organising a cyclical file comprising the steps
18 of dividing the file into a plurality of regions, further dividing each
19 region into a plurality of blocks of equal length, each block including
20 a chaining number, initially storing records sequentially beginning in
21 the first block in each desired region while recording in the chain
22 number portion of each following block the number of the first block
23 wherein the record is recorded, purging selected records from the
24 file by effectively erasing each block wherein the record to be purged
25 is located, and recording further records in the file beginning in the
26 first available block in the region and sequentially thereafter in sub-
27 sequent available blocks as needed and recording in the chain number
28 portion of each of the blocks the number of the first block wherein the
29 record is recorded.

30 Further, in accordance with the present invention, there

1 is provided a data storage system for storing data records comprising a cyclical data storage medium divided into a plurality of regions of selected lengths, each region being divided into a plurality of blocks; means mounted for reading data on the data storage medium; writing means mounted behind the reading means for subsequently writing data on the data storage medium; region detection means for detecting the start of a selected region and resetting and rendering the system effective upon making such detection; gateable buffer means for temporarily storing data records to be written; the output thereof being connected to the writing means; block detection means 10 responsive to the reading means for detecting whether a block is empty; block indication means responsive to the operation of the detection means for storing a chaining character representative of the first detected empty block and for operating the writing means to write that character at the beginning of the first and each subsequently detected empty block; gating means responsive to operation of the detection means for gating the buffer means to thereby supply data to the writing means between the chaining character and the end of the block; and termination means for detecting the end of the data record being written to terminate the operation of the block indication means and gating means.

20 The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention, as illustrated in the accompanying drawings, in which:

Fig. 1 is an overall block diagram of the principal components of a data processing system incorporating the invention;

Fig. 2 schematically illustrates a block of data recorded on a cyclic file incorporating the invention;

28 Figs. 3a, 3b and 3c schematically illustrate data from various records as distributed in various blocks on the cyclic file in accordance with

1 the present invention; and

2 Figs. 4A and 4B, when arranged side-by-side, comprise
3 Fig. 4 which schematically illustrates in block diagram form the
4 electrical circuitry for carrying out the present invention.

5 DATA STORAGE METHOD

6 Referring to Fig. 1, a data processing system is shown
7 including, interalia, a central processing unit 10, a file control unit 11
8 and a cyclic file 12, each interconnected by means of various cables.
9 The central processing unit is a complete system or a portion of a
10 system that utilizes data from cyclic file 12 and which is capable of
11 cooperating with the file by writing data thereto, reading or purging
12 data therefrom, or reading data for the purpose of changing or updating
13 the data and writing it back into the cyclic file.

14 The cyclic file 12 may be any well-known magnetic drum
15 unit, any well-known magnetic disk unit or any other similar type of
16 cyclic file. The file control unit 11 comprises electronic circuitry for
17 interpreting the commands from the central processing unit and re-
18 sponding by causing cyclic file 12 to perform the desired operation.

19 For the purpose of illustration, cyclic file 12 is assumed
20 to be a rotating drum unit of any type presently on the market. The
21 drum is preferably divided into a plurality of parallel tracks, each
22 extending circumferentially around the drum.

23 The drum may be organized into a plurality of regions,
24 each of which may for the purpose of illustration comprise a selected
25 number of tracks along the drum. The CPU selects the desired region
26 by transmitting a set of logical signals on track select cable 15 to the
27 file control unit, which selects the desired track with signals on control
28 line 16.

29 Referring to Fig. 2, any embodiment of my method of
30 storing data must be dependent, not only upon the method, but also

1 upon the format selected for the data. The format selected may vary
2 from a complete freedom of timing or length considerations, utilizing
3 special control characters to designate the beginning of data, etc., to
4 a very strict position and length format without control characters.

5 Fig. 2 illustrates a format which is somewhat of a com-
6 promise to simplify the circuitry involved in the illustrated system.

7 As shown in Fig. 2, each region is divided into a region
8 start character 20 and a plurality of equal length blocks 21. The region
9 start character 20 is a special character which indicates the beginning
10 of a region. The character is previously recorded, either by conven-
11 tional recording techniques, or, alternatively, may comprise a
12 permanent recording made of miniature magnetic slugs or other means.

13 Each block 21 includes a previously recorded start character
14 22 which indicates the beginning of the block. The start characters are
15 so spaced that each block contains an identical number of bits of data.
16 These start characters may be recorded by normal recording techniques
17 or alternative means in the same manner as region start character 20.
18 Following the start character, there appears a series of normally
19 recorded data bits. The first of this data comprises a status character
20 23 which, as will be explained hereinafter, comprises a character
21 representing whether the remainder of the block has data therein or is
22 empty. The following characters represent a chain number 24 which
23 will be explained hereinafter. The following bits 25 represent stored
24 data which may or may not include an end of record character 26.

25 Certain practical observations have been made with respect
26 to the normal type of data that is stored for future reference in practical
27 systems. The first observation is that each usable unit of data in its
28 most convenient form, called a record, is not of identical length; as a
29 matter of fact, considerable variation will normally occur.

30 The second practical observation is that any convenient

1 gross organisation of data relating to the contents thereof will result
2 in an unequal number of records within each division, called a region.
3 For example, in a dictionary with thumb index notches cut at each
4 letter, the number of entries between notches has large variation. In
5 addition, the length of entries varies considerably. A further example
6 is an encyclopedia where entries vary from a few paragraphs to many
7 pages.

8 If it is desired to prevent the wastage of available storage
9 space, some way must be found to correlate the actual region and
10 record lengths with the expectancy of probable data lengths.

11 With respect to record lengths, the illustrated system
12 embodying the present method reduces wastage substantially by making
13 the data areas 25 of the data block 21 substantially shorter than the
14 average length of expected data records. For example, the data area
15 is fifty characters in length. Thus, a data record is stored by chaining
16 the number of blocks needed to store all of the data contained in the
17 data record. The chain numbers 24 of the individual blocks making up
18 a particular record are automatically made identical so as to keep
19 track of the blocks on which the record is stored. The last block in the
20 chain is denoted by the appearance in the data area 25 therein of an
21 end of record character 26.

22 To accommodate the difference in region lengths, another
23 observation concerning data has been made. The observation is that,
24 assuming the total amount of data stored in the storage system remains
25 approximately the same, the amount of data contained in any one region
26 will not vary significantly over a period of time. For example, although
27 people move into and out of a city thereby changing the actual listings
28 in the telephone directory, the proportion of people in the city having
29 names beginning with a particular letter of the alphabet will tend to
30 remain approximately the same.

1 Therefore, an analysis of the data to be stored is made
2 and the regions selected. The approximate lengths of the regions are
3 then estimated in accordance with the above analysis and the regions
4 located on the cyclic file 12 accordingly. Thus, the region start
5 symbol 20 is recorded at the beginning of each region and the addresses
6 thereof to be selected by the file control unit 11 stored in the file
7 control unit 11 or in a relatively small auxiliary memory for use in
8 programming. As will be seen, the sole addressing to concern the
9 programmer will be that of seeking and finding a particular region,
10 such as a region of surnames beginning with alphabetic character "A",
11 which would be called the "A" region. From that point on, the method
12 and apparatus of the present invention will retrieve or write all data
13 of a particular record automatically without knowledge or concern of
14 the programmer.

15 In summary, the total memory is divided into a large
16 number of regions, and each region is further divided into blocks 21
17 having data areas 25 of, for instance, fifty characters. Records to be
18 stored are variable in length and may comprise any number of charac-
19 ters extending to any number of blocks in length. Since the record may
20 extend over a number of blocks, the chain number 24 of each of the
21 individual blocks making up a particular record are identical. Each
22 record terminates in an end of record character 26 and the appearance
23 thereof in the data portion 25 of a block thereby denotes that it is the
24 last block containing the record.

25 Referring now to Figs. 3A-C, an example of chaining and
26 the use of the chain number 24 with respect to the subject method is
27 described. Preferably, the system is designed to write in the first
28 block indicated as being empty and subsequent data of a record is
29 recorded and chained in following available blocks. Since an immedi-
30 ately subsequent block may be full and cannot be written over, those

1 blocks must be skipped before writing of data is resumed in empty
2 blocks. Chaining is therefore required to keep track of the blocks
3 containing a particular record.

4 In Fig. 3A it is assumed that the complete region was
5 empty except for the region start and block start symbols 20 and 22.
6 It is further assumed that seven records are written sequentially into
7 the region. To simplify the example of the invention, one record will
8 be completely written for each complete cycle of the memory. For
9 convenience in keeping track of particular records in explaining the
10 example of Fig. 3, each record is assigned a specific number. In
11 practice, there is no necessity to so designate each record since the
12 chain number automatically keeps track of the record even though it
13 may be distributed throughout a region.

14 Thus, in Fig. 3A seven records are stored. Record no. 1
15 is three blocks in length and therefore is stored in block nos. 1, 2 and
16 3. Record no. 2 is two blocks in length and is stored in block nos. 4
17 and 5, while record no. 3, which is five blocks in length, is stored in
18 block nos. 6-10, etc. Each record thus continues in sequentially
19 adjacent blocks and chaining is not necessary since no blocks are to be
20 skipped. A complete record may be read by merely continuously
21 reading data until an end of record character is detected.

22 The method to be utilized in practice normally determines
23 and writes chain numbers even when no blocks are skipped since
24 whether any will be skipped is not known in advance. Thus, record
25 no. 1 begins in block no. 1 and this becomes the chain number for that
26 record. Similarly, record no. 2 begins in block no. 4, so "4" becomes
27 the chain number for that record, etc.

28 Referring to Fig. 3B, record no. 2 is purged and a new
29 record, no. 8, is stored in the memory.

30 As will be described with respect to the system, chaining

1 means are provided for counting or keeping track of the individual
2 block numbers until the desired record is located if a record is to be
3 purged or read, or until the first empty block is located if a record is
4 to be written. The number of the first block so located is the chain
5 number for either the record to be purged or read or of the record to
6 be written.

7 Referring additionally to Fig. 1, to purge record no. 2 in
8 accordance with the subject method, the CPU energizes command purge
9 line 34 and command read line 43. The data from block no. 1 is then
10 read out on cables 30 and 31 to CPU 10 for its program 32 to determine
11 whether the data denotes the desired record. Since the desired record
12 is record no. 2, no comparison is made and the CPU provides an out-
13 put signal on reject line 33. This causes the system to then read the
14 data from the next block having a chain number and block number which
15 are identical, which is block no. 4. Then, a comparison is made by
16 the program 32 and no reject signal is transmitted on line 33. The
17 lack of a reject signal on line 33 together with a command purge signal
18 of two-character duration on line 34 causes the status character 23 of
19 block no. 4 to be altered from "full" to "empty". Block no. 5 will
20 have the same chain number as block no. 4 and therefore is purged
21 automatically, upon matching the chain number, by altering the status
22 character. The purging is ceased by detection of end of record symbol
23 within the data area 25 of block no. 5.

24 The new condition present in Fig. 3B is that record no. 2
25 was merely two blocks in length whereas record no. 8 is four blocks
26 in length. Therefore, record no. 8 cannot be written completely in
27 consecutively adjacent blocks and some blocks must be skipped.

28 In storing record no. 8, the system detects whether each
29 block is empty or full and when it comes to the first empty block, which
30 in this case is block no. 4, it begins to store the new record. Thus,

1 the first two blocks of record no. 8 are stored in block nos. 4 and 5.
2 The system detects that the following blocks are full so it does not
3 write. The system then looks for the next empty block, which in this
4 case is block no. 22, followed by block no. 23, wherein the two
5 remaining blocks of record no. 8 are then stored. The particular
6 organisation shown, therefore, always tends to pack data towards the
7 front, denoted by the region start character 20.

8 Specifically, on a subsequent cycle of the memory after
9 record no. 2 is purged, record no. 8 is written into storage. This is
10 accomplished by writing data into file control unit 11 on line 40 and
11 energising the command write line 41. The system will then wait for
12 the arrival of the first block having a status character 23 indicating
13 that the block is "empty". Block nos. 1, 2 and 3 are indicated as
14 being "full". Block no. 4, however, is now indicated as being "empty".
15 Immediately, the number of that block is written as chain number 24
16 within the block and the data of record no. 8 is written via write cable 42
17 in data-area 25 of block no. 4.

18 The writing of the data is stopped at the end of data area 25
19 and the search continued for another empty block. In this case, block
20 no. 5 is also empty, so that the block number of the first block con-
21 taining data from record no. 8, which is block no. 4, is written as the
22 chain number of block no. 5. Then, additional data of record no. 8 will
23 be written in data area 25 of block no. 5. Upon reaching the end of
24 data area 25, the search for the next empty block continues. Block
25 nos. 6-21 will all be indicated as "full", and block no. 22 is the first
26 empty block. Therefore, number 4 is written as the chain number in
27 block no. 22 and additional data from record no. 8 written in data area
28 25 thereof. Block no. 23 is also empty so chain number 4 will again be
29 written and the remaining data of record no. 8 written therein including
30 end of record character 26. Writing end of record character 26 ceases

1 further operation of the system for seeking empty blocks.

2 Therefore, the data of record no. 8 has been automatically
3 written in the first available empty blocks thereby packing data to the
4 front and a simple chaining number automatically generated for keeping
5 track of the record.

6 Still referring to Figs. 1 and 3B, an example of reading
7 the data of record no. 8 is illustrated. The program 32 of the CPU 10
8 causes the CPU to select the desired track and to transmit a signal on
9 command read line 43 to file control unit 11. The file control unit
10 responds by causing the data from block no. 1 to be read out on cables
11 30 and 31 since it is the first block of a record. The CPU receives the
12 data and its program determines whether the desired data is being read.
13 Since the desired record is no. 8, no comparison is made and the CPU
14 provides an output signal on reject line 33. This causes the system to
15 then skip block nos. 2 and 3 since they are not the first blocks of a
16 record. Block no. 4 is then read and the program indicates that the
17 desired record has been located and no reject signal is transmitted.
18 This establishes block no. 4 as the chain number so that the system
19 automatically reads out the data of block no. 5, skips block nos. 6-21
20 and reads the data of block nos. 22 and 23. The end of record character
21 present in the data area of block no. 23 causes the system to cease
22 transmission of data.

23 Thus, the CPU merely selects desired data and, once the
24 selection has been made, the system automatically transmits on cable 30
25 only the data comprising the remainder of the selected record.

26 Fig. 3C illustrates merely a continuation of the above
27 described method wherein record no. 1 contained in block nos. 1-3
28 has been purged therefrom and record no. 9 inserted in block nos. 1-3
29 and 24 with chain number 1, which represents the first block in which
30 data from record no. 9 is written.

1 At any time when data is entered into an empty block, the
2 system automatically rewrites the status character 23 as "full" before
3 writing the chain number or data. Thus, it is seen that no actual
4 erasure of data need occur since the status character 23 alone indicates
5 whether a block is empty or full.

6 It is therefore seen that the desired method of organizing a
7 cyclical file includes the steps of dividing the file 12 into a plurality of
8 regions, further dividing each region into a plurality of blocks 21,
9 initially storing records sequentially beginning in the first block of the
10 desired region and recording the number of the first block in the chain
11 number position 24 of each following block in which the record is
12 recorded, purging the selected records from the file by selectively
13 erasing each block wherein the record to be purged is located as defined
14 by the chain number, and recording further records in the file begin-
15 ning in the first available block of the desired region and sequentially
16 thereafter in the subsequent available blocks and again recording the
17 number of the first block wherein the record is recorded in the chain
18 number portion of each of the subsequent blocks.

19 The above method is not restricted to any particular format.
20 In the example shown, the sequence and lengths of characters and data
21 are fixed. However, as will be explained, they need not be for the
22 above method to operate. Alternatively, additional control characters,
23 such as "chain number follows" wherein the chain number always
24 immediately follows this character, may be used to control operation
25 of a system embodying the subject method.

26 FILE SYSTEM

27 Referring now to Fig. 4, an example of a system for
28 accomplishing the steps of the above method is shown. As an example,
29 the cyclic file shown comprises a drum 100, read head 101, and write
30 head 102. As previously stated, the drum unit may be of any commercially

1 available type. Although the drum unit is shown with only two heads 101
2 and 102, all presently available units utilize a plurality of heads which
3 either are stationary, thereby requiring one set of heads for each track,
4 or which physically move the heads from position to position to trace
5 out a plurality of tracks. In either case switching is required between
6 the various sets of heads so as to communicate with all of the desired
7 tracks. The schematic diagram shown in Fig. 4 is therefore meant to
8 include any of the schemes and the illustration is merely of a single
9 pair of heads communicating with a selected region which comprises
10 merely a single track 103 as defined by the set of heads 101 and 102.

11 The drum circulates counter-clockwise, as shown by arrow
12 104, so that read head 101 reads the data before it appears under write
13 head 102. The distance therebetween must amount to at least one
14 character in length, but less than one block in length. Not all of the
15 presently available drum units are so constructed; therefore, those
16 particular units must be modified slightly to be used with the system as
17 illustrated.

18 Within the drum unit, read head 101 is connected to a read
19 amplifier 105 and write head 102 is connected to a write amplifier 106.
20 These merely amplify and properly compensate the signals for proper
21 reading or recording.

22 In Fig. 1, file control unit 11 and cyclic file 12 are shown
23 as separate units. This is in keeping with the recently developed con-
24 cept of separate file control units. However, the subject invention is
25 equally well adapted to be incorporated in a file control unit contained
26 within the cabinet of a cyclic file 12.

27 The normal file control unit contains a deserializer 110 which
28 is connected to read amplifier 105 and a serializer 111 which is connected
29 to write amplifier 106. Most of the presently available drum units store
30 data in the serial by bit, serial by character form, whereas most digital

1 computing systems utilise digital data in the parallel by bit, serial by
2 character form. Thus, deserializer 110 accepts a serial string of
3 data from read amplifier 105 and stores the same until sufficient data
4 is received to make up a complete coded character comprising, for
5 example, seven bits. Deserializer 110 then transmits this character
6 on a cable which contains, for example, seven wires. In Fig. 4, all
7 of the heavy lines are such cables and all of the light lines comprise
8 single wires. Serializer 111 does the opposite and converts characters
9 of parallel bits into characters of serial bits.

10 A single character register 112 is connected to deserializer
11 110 to receive the parallel data therefrom after a character has been
12 deserialized and then stores the character until the next character has
13 been deserialized. At this time, the register is reset by a clock pulse
14 and the new character read in. The output of the register therefore
15 comprises a single character lasting for one character period (the time
16 required to deserialize a character).

17 All of the remaining circuitry shown in Fig. 4 is equipment
18 which must be added to the standard file control unit 11 of Fig. 2. The
19 clocking pulses utilised to drive the circuitry of Fig. 4 may be obtained
20 from the standard clock sources for the file control unit.

21 WRITE CIRCUITRY

22 As described with respect to Figs. 1-3, the CPU 10 writes
23 data by transmitting the data on cable 40 and by transmitting a com-
24 mand write signal on line 41, both to the file control unit 11. The CPU
25 and its program have nothing more to do with the data to be written;
26 rather, the actual storage of data, including packing the data toward
27 the front, is automatically accomplished by the system of the subject
28 invention.

29 According to the above method, the system stores the data
30 temporarily, detects whether each block is empty or full, and when it

1 comes to the first empty block, it begins to store the new record.
2 The remainder of the record is then stored in each subsequently
3 available empty block until the end of record is reached which is
4 denoted by end of record character 26. Additional functions include
5 the changing of the status character 23 of each block in which data is
6 entered from "empty" to "full" and the establishment of a chaining
7 number 24 which denotes all blocks containing the particular record.

8 Referring now to Fig. 4, when the CPU transmits data on
9 cable 40, it is received in an input buffer register 120. The input
10 buffer register is of sufficient capacity to hold the longest record to
11 be transmitted by CPU 10. The register is of the shifting type and
12 the input data is gated such that the first character thereof appears in
13 the first stage of the buffer, the second character in the second stage,
14 etc. When a positive signal appears on READOUT input 121, the
15 register shifts under the control of a clock source synchronized by the
16 drum 100 so as to transmit one character at a time through OR circuit
17 122 to serializer 111 beginning with the character in the first stage of
18 the buffer register. The transmission to serializer 111 continues so
19 long as a signal appears on READOUT input 121. The clock rate for
20 controlling the shifting of the register is such that serializer 111 is
21 able to serialize the data to write amplifier 106 and write head 102
22 at the proper bit rate as determined by the rotational speed of drum 100.

23 The command write signal on line 41 operates a latch
24 circuit (not shown) which in turn operates switches 130-137 to the "W"
25 or "write" position. The latch remains on until such time as the CPU
26 transmits either a command read or a command purge signal.

27 As previously stated, the data on track 103 of drum 100 is
28 continually read by read head 101 and read amplifier 105. This data is
29 transmitted to deserializer 110 which converts the data into parallel
30 characters for transmission to single character register 112. The

1 Register stores the data representing one character for the duration of
2 a single character time. Meanwhile, during this single character
3 time, the deserializer is converting the subsequent character into
4 parallel form.

5 The data stored by the register appears on the parallel
6 lines of cable 140 which is connected to gate circuit 141, detect region
7 start circuit 142, detect block start circuit 143, gate circuit 144 and
8 switch 132.

9 Detect region start circuit 142 detects the region start
10 character when it appears in parallel form on cable 140. This circuit
11 is a standard logic circuit arranged to provide an output only upon the
12 receipt on cable 140 of electrical signals comprising the unique bit
13 combination making up the region start character. This output is
14 provided on line 150 and lasts as long as the region start character
15 remains on cable 140, which is the one character duration of single
16 character register 112.

17 Line 150 is connected to the RESET input of block counter
18 151, to OR circuit 152, the SET ON input of purge blocking flip-flop
19 153, the SET ON input of write complete flip-flop 154, and to the
20 RESET input of purge register 155.

21 As will be explained hereinafter, the function of block
22 counter 151 is to count the number of blocks detected until the first
23 available empty block is found. The resultant count is then utilized
24 as the chain number. Therefore, it is necessary that the counter be
25 reset to zero at the beginning of the region so that its count of blocks
26 may begin at that point. The appearance of a pulse on line 150 as a
27 result of detecting the region start character accomplishes this
28 resetting of the counter.

29 A signal appearing on line 150 is transmitted by OR circuit
30 152 to the SET ON input to block counter flip-flop 156. The block

1 counter flip-flop, as will be explained hereinafter, controls AND
2 circuit 157 to gate block start signals until an empty block is detected.

3 Thus, the block counter will contain the number of the block in which
4 the recording of data is begun.

5 The basic function of the region start character is therefore
6 to reset the entire system so that it is ready to perform the proper
7 function as commanded by the CPU.

8 Detect block start circuit 143 is a logic circuit for detecting
9 the block start character and supplying an output signal on line 160 in
10 response thereto. The detect block start circuit is a circuit similar
11 to the detect region start circuit 142 in that it is logically arranged to
12 detect the combination of bits appearing on cable 140 which comprise
13 the block start character. The output of the circuit is a voltage level
14 which lasts for the duration of the appearance of a block start character
15 at the output of single character register 112. The output line 160 is
16 connected to the SET ON input of status flip-flop 161, one character
17 single shot circuit 162 and AND circuit 157.

18 The format arbitrarily used in Fig. 2 for blocks places the
19 status character immediately after the block start character. Therefore,
20 status flip-flop 161 and one character single shot circuit 162 are
21 arranged to utilize the detection of the block start character to
22 gate 144 for one character time immediately following the end of the
23 block start signal on line 160.

24 The SET ON and SET OFF inputs to status flip-flop 161 and
25 the input to one character single shot 162 all include a differentiating
26 network which responds to the negative-going portion of a positive pulse.
27 Thus, since the positive pulse appearing at the output of detect block
28 start circuit 143 is of duration of a single character time as determined
29 by single character register 112, the SET ON input to status
30 flip-flop 161 and the input to one character single shot 162 are both

1. operated as detect block start circuit 143 turns off.
2. One character single shot 162 thereby provides a positive
3. output on line 163 for the time duration of the single shot which is set
4. to be slightly longer than one character time. This signal has no
5. effect on status flip-flop 161 since the SET OFF input thereto responds
6. only to the negative-going portion of the signal.

7. The negative-going portion of the output from detect block
8. start circuit 143 sets on status flip-flop 161 so that it operates gate 144,
9. which remains open, so long as the signal on line 163 remains positive.
10. Slightly more than one character time later, single shot 162 turns off.
11. The negative-going portion of its output signal causes status flip-flop
12. 161 to turn off so as to turn off gate 144, blocking any further characters
13. appearing on cable 140.

14. At the time gate 144 was opened by status flip-flop 161,
15. single character register 112 concluded transmission of the block
16. start character and received the status character from deserialiser 110.
17. This character is stored by the register for one character time during
18. which the character is transmitted on cable 140. Gate 144, having been
19. operated by status flip-flop 161, transmits the status character over
20. cable 170 to detect status full circuit 171 and detect status empty
21. circuit 172. At the conclusion of transmission of the status character,
22. flip-flop 161 closes the gate and blocks transmission of further charac-
23. ters by the gate.

24. Circuits 171 and 172 are straightforward logic circuits
25. similar to detect region start circuit 142. Circuit 171 responds to the
26. signals appearing on cable 170 comprising the status full character
27. and responds by providing an output on line 180. Circuit 172 similarly
28. detects the arrangement of signals on cable 170 representing the status
29. empty character and responds by providing an output on line 181.

30. The present system is designed to write a record in the

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1 first available empty block and to cease writing after the end of record
2 symbol has been detected. It is probable that, on some occasion, the
3 CPU will write new data into the input buffer register 120 before the
4 previous cycle of the drum has been completed. Therefore, it is
5 necessary to prevent the detection of status empty characters from
6 causing the system to write an incoming new record into storage until a
7 new cycle of the drum has begun, as indicated by a region start character.

8 The above is accomplished by write complete flip-flop 154
9 and AND circuit 158. Write complete flip-flop 154 is turned on by the
10 appearance of a pulse on line 150 indicating the detection of the region
11 start character by circuit 142. This, in turn, provides one input to
12 AND circuit 158. The flip-flop is turned off by the appearance of a
13 pulse on line 182 which indicates that an end of record character has
14 been detected, as will be explained hereinafter.

15 Thus, write complete flip-flop 154 is turned on at the
16 beginning of a region so as to provide one input to AND circuit 158 and
17 thereby gate signals from detect status empty circuit 172 appearing on
18 line 181 to switch 136 until an end of record character has been detected.
19 By this means the flip-flop 154 controls the gating of the output of
20 detect status empty circuit 172 such that the detection of status empty
21 characters operates to write additional data only until the end of record
22 character of the record being written has been detected preventing the
23 writing of any additional data.

24 Switch 136 is in the write position thereby allowing signals
25 gated by AND circuit 158 to appear on line 190. Line 190 is connected
26 to switches 131 and 192, to the SET OFF input of block counter flip-
27 flop 156, and to one character delay 191.

28 Switch 131 is thrown into the write position transmitting
29 status empty signals to set status full circuit 20ⁿ and OR circuit 201.

30 An object of the system is to skip all blocks indicated as

being full and write data in the first available blocks. Therefore, it is necessary to change the status character in each block in which data is written from "empty" to "full". To accomplish this the output of detect status empty circuit 172 is used to operate set status full circuit 200. The set status full circuit comprises a plurality of single shot circuits connected to selected lines of cable 202. The combination of signals on these lines as generated by the single shot circuits comprises the status full character. The single shots are actuated by the appearance of a pulse on line 190 and provide outputs lasting for a sufficient period of time to be transmitted by OR circuit 203 to single character register 204 and to set the register with the status full character.

Single character register 204 comprises a parallel storage register made up of a plurality of flip-flops and also comprising a plurality of AND gates, each associated with the output of a flip-flop. The SET ON inputs to the flip-flops are connected to the wires coming from OR circuit 203. The SET OFF inputs to the flip-flops and the control inputs to the AND gates are both connected to command readout line 205. The SET OFF inputs to the flip-flops include differentiating circuits causing the flip-flops to turn off as a result of the negative-going portion of a positive pulse received from line 205.

Therefore, data appearing at the SET ON inputs to the flip-flops from OR circuit 203 turns on selected ones of the flip-flops. The subsequent pulse appearing on command readout line 205 operates the AND gates to transmit the data from the flip-flops to cable 206. The signals remain on the wires comprising cable 206 until the pulse on line 205 ends turning off the AND gates. The negative-going portion of the pulse on line 205 also operates the SET OFF inputs to the flip-flops thereby resetting the register.

30

The same pulse that operates set status full circuit 200 is

1 transmitted by OR circuit 201 to head delay and single shot circuit 207. The head delay and single shot circuit 207 comprises two serially arranged single shot circuits. The first single shot has an output which is normally on and the circuit responds to the appearance of a pulse from OR circuit 201 by turning off for a specified time period. This time period is selected to equal the delay time between the appearance of a pulse thereto as a result of reading a status character with read head 101 and the appearance of the beginning of that status character under write head 102, less the time delay due to operation of register 204, serializer 111 and amplifier 106. This time period will be the same for each block recorded on drum 100 and allows the detection of a status character to control the writing of the new status character in the same physical position on the drum. At the end of the time period, the first single shot returns to its normally on state, thereby operating the second single shot. The second single shot responds to the positive-going portion of the output from the first single shot by providing a positive output pulse one character time in length at its output. This output is transmitted to one character delay circuit 208 and to single character register 204 on command readout line 205.

20 Therefore head delay and single shot circuit 207 controls single character register 204 to gate the output of the register to serializer 111 for one character time during which time the status character that operated detect status empty circuit 172 is under write head 102 so as to thereby alter the character from "empty" to "full".

30 As stated previously, block counter flip-flop 156 controls AND circuit 157 to gate block start signals to block counter 151 until an empty block is detected. Thus, the block counter counts the block start signal of every full block and of the first empty block so that it then contains the number of the block in which the recording of data is begun.

1 Block counter 151 comprises a conventional set of four
2 stacked ring counters, each representing a digital order of magnitude.
3 The output of each stage of each counter is properly coded and con-
4 nected to the same set of parallel wires by means of OR circuits.
5 Each one of the resultant four sets of lines is connected to a gate
6 circuit and the gate circuits are connected through OR circuits to
7 cable 210. The gating inputs of the gate circuits are connected to
8 various stages of a stepping circuit, which operates at the character
9 rate. The stepping circuit comprises five stages, the first stage
10 being connected to the gate circuits connected to the outputs of the
11 highest ordered counter, etc., and the fifth stage is a rest stage not
12 connected to any lines.

13 The GATE input to the block counter is connected so as to
14 turn off the rest stage of the stepping circuit and to turn on the first
15 stage. The first stage remains on for one character time and then
16 turns off and turns the second stage on. The stepping continues until
17 the rest stage is turned on. The rest stage then remains on until
18 again activated by pulse on the GATE input to the block counter.

19 To obtain the proper chain number, therefore, the region
20 start signal appearing on line 150 operates the RESET input to block
21 counter 151 to thereby reset the counter to zero and also appears at
22 the SET ON input of block counter flip-flop 156 to thereby turn the
23 flip-flop on. The output of the flip-flop thus provides one input to
24 AND circuit 157 thereby gating subsequent block start signals appearing
25 on line 160 to the COUNT input of the block counter 151. The counter
26 counts each such pulse so received and retains the cumulative count
27 until again reset.

28 As previously stated, the negative-going portion of the
29 output of detect block start circuit 143 turns status flip-flop 161 on.
30 The output of this flip-flop is connected to the GATE input to block

counter 151. Therefore, immediately upon counting the block start pulse from line 160, the pulse from status flip-flop 161 starts the stepping circuit to transmit the count registered by the counter onto cable 210. The number comprises four sequential characters, each being transmitted for one character time.

The block counter flip-flop 156 remains on and the block counter 151 continues counting so long as each block is full. As the first empty block appears at read head 101, its block start character is detected by circuit 143 and the resultant pulse on line 160 is counted by block counter 151. Subsequently, its status character is detected by detect status empty circuit 172 and a pulse transmitted on line 190 to appear at the SET OFF input to block counter flip-flop 156. This pulse turns the counter off thereby removing one input to AND circuit 157. This prevents any further block start pulses from reaching the COUNT input to block counter 151 until the next region start character is detected. Therefore, block counter 151 retains as its output the number of the first available block having a status character which indicates that the block is empty. This is the number of the first block in which data is written and constitutes the chain number for all following blocks in which data from the particular record is being written.

The output of the block counter is connected to compare block count and chain number circuit 211 and also to switch 133.

The object of obtaining the chain number in block counter 151 is to write the chain number in all blocks in which the particular record is written. Therefore, the predetermined delay of head delay and single shot circuit 207 is utilized to control the writing of the chain number into each block immediately after the status full character is written therein. Thus, the output of head delay and single shot circuit 207 is connected to one character delay circuit 208. The delay

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1 circuit comprises any suitable delay means for duplicating at its output
2 a pulse received at its input one character time later. The purpose of
3 this delay is to provide a pulse for writing the chain number one
4 character time after the beginning of writing the status full character.

5 One character delay circuit 208 is connected through switch
6 130, which is in the write position, and line 214 to the GATE input of
7 block counter 151 and to four character delay 215. After head delay
8 and single shot circuit 207 provides an output on command readout line
9 205 to transmit the set status full character to be written in the status
10 position, one character delay 208 delays this pulse for one character
11 time, during which the status character is being written, and transmits
12 the pulse through switch 130 to the GATE input of block counter 151.
13 The pulse then operates the stepping circuit so as to gate the chain
14 number onto cable 210.

15 Cable 210 is connected to compare block count and chain
16 number circuit 211, to compare chain number and purge register
17 circuit 217, and to switch 133. Switch 133 is set in the write position
18 thereby transmitting the chain number through OR circuit 122 to
19 serializer 111. The serializer serializes each of the four characters
20 sequentially and transmits the serial data to write amplifier 106 which
21 writes the data, via head 102, into the chain number position of the
22 block.

23 Therefore, the block counter keeps track of the number of
24 block start characters detected until, and including, that of the first
25 detected empty block, and head delay and single shot circuit 207 and
26 one character delay 208 gate the number through serializer 111 and
27 write amplifier 106 to write head 102 so as to write the number in the
28 chain number position of the first available empty block. Block counter
29 flip-flop 156 then blocks AND circuit 157 to prevent the block counter
30 151 from counting any additional block start characters.

1 In each additional empty block detected before the detection
2 of the end of record symbol of the data being written, as controlled by
3 write complete flip-flop 154, detect status empty circuit 172 operates
4 head delay and single shot 207 and one character delay 208 to again
5 gain the chain number from block counter 191 to write head 102 so as
6 to thereby write the chain number into each additional block until the
7 record has completely been written into storage.

8 After generating and writing the chain number into a block,
9 the next step is to write the proper amount of data into the data area
10 of each empty block until the end of record character is detected and
11 written.

12 As stated above, the output of head delay and single shot 207
13 and one character delay 208 is transmitted by switch 130 and line 214
14 to four character delay 215. Four character delay 215 is similar to
15 one character delay 208 and comprises means for accurately delaying
16 a gating signal for four clocked character times.

17 Delay 215 is connected through switch 137, which is in the
18 "W" position, and OR circuit 220 to the SET ON input to block length
19 flip-flop 221. The flip-flop is of conventional construction and, when
20 turned on by a pulse from delay 215, produces an output on line 222.
21 This output remains on until the flip-flop is subsequently turned off,
22 as will be explained hereinafter. The output line 222 is connected to
23 one input of AND circuit 223 and to switch 134. Switch 134 is in the
24 write position thereby transmitting the output signal from the flip-flop
25 onto line 121 to the READOUT input of input buffer register 120,
26 thereby causing the register to transmit the data therein through OR
27 circuit 122 to serialiser 111.

28 Thus, for each block in which data is written, the output
29 of one character delay circuit 208 is delayed four additional character
30 times by four character delay 215 during which time the chain number

1 is written into the chain number portion of the block. Then, delay 215
2 turns on block length flip-flop 221 which operates input buffer register
3 120 to transmit data to serialiser 111. The register is controlled by
4 the character clock of the file control unit so as to transmit one character
5 of data for one character time, then to shift the data therein and trans-
6 mit a second data character for one character time, etc. Serialiser 111
7 serialises these characters and transmits the serial data through write
8 amplifier 106 to write head 102 where the data is written in the data
9 area of the block.

10 As stated above, the output of block length flip-flop 221 is
11 connected, via line 222, to one input of AND circuit 223. The other
12 input to the AND circuit comprises the output of the character clock
13 of the file control unit. Thus, while block length flip-flop 221 is on,
14 the character clock pulses are gated through AND circuit 223 to the
15 COUNT input of block length counter 224. The block length counter
16 comprises a conventional binary counter wherein the output is connected
17 to OR circuit 225. The counter is set to count a predetermined number
18 of pulses equivalent to the number of characters in the data area of
19 each block before producing output. The final stage is unstable and
20 provides an output pulse one character time in length and then switches
21 returning the counter to the "0" or "rest" stage of the counter.

22 Thus, the counter counts the number of characters in the
23 data area of each block and then provides an output signal of one
24 character time duration. This output is transmitted through OR
25 circuit 225 to the OFF input of block length flip-flop 221 thereby
26 turning the flip-flop off. As the flip-flop is turned off, it removes the
27 input to AND circuit 223 thereby blocking further character clock pulses
28 from the block length counter 224. The turning off of the block length
29 flip-flop 221 also removes the signal from the READOUT input to input
30 buffer register 120 thereby stopping further transmission of data to
31 serialiser 111.

1 In this manner, the output of one character delay 208
2 operates flip-flop 221 to begin transmission of data from input buffer
3 register 120 and simultaneously gates character clock pulses to block
4 length counter 224. The counter counts the number of characters in
5 the data area and then turns off the flip-flop to end the transmission
6 of data to serialiser 111.

7 Detection of the next block start character by detect block
8 start circuit 143 provides a pulse on line 160 which resets the block
9 length counter to zero. The counter is thereby placed in condition to
10 begin counting the next time flip-flop 221 is turned on.

11 At one point, the end of record character appended to the
12 data being written will be detected. This requires an immediate
13 cessation of writing so that no data from a following record is trans-
14 mitted until the next revolution of the drum.

15 The output of the input buffer register is connected through
16 OR circuit 230 to detect end of record circuit 231. Circuit 231 com-
17 prises a conventional logic circuit similar to detect region start
18 circuit 162, which is arranged to respond to the data bits comprising
19 the end of record character by providing an output on line 182. This
20 output lasts as long as the end of record character is maintained on
21 either of the input lines to OR circuit 230 which is one character time.
22 Output line 182 is connected to the SET OFF input to write complete
23 flip-flop 154, which operates as previously explained, through OR
24 circuit 223 to the SET OFF input to block length flip-flop 221, and to
25 the RESET input of block length counter 224.

26 As previously stated, the output of the block length flip-flop
27 controls the character clock input to block length counter 224. Thus,
28 as input buffer register 120 transmits the final character of a record
29 to serialiser 111, the character is also transmitted by OR circuit 230
30 to detect end of record circuit 231. The circuit detects the end of

1 record character and provides an output on line 182, thereby turning
2 off the block length flip-flop 221. This turns off the signal on line 222
3 which appears at the READOUT input to the input buffer register.
4 thereby terminating the transmission of data by the register.

5 Since block length flip-flop 221 was turned off, blocking
6 the transmission of further character clock pulses through AND circuit
7 223, block length counter 224 must be reset without counting to the
8 final stage. Thus, the output of detect end of record circuit 231 is
9 used to operate the RESET input of the counter, resetting the counter
10 to the "0" or "rest" stage.

11 Block length flip-flop 221 is prevented from turning on for
12 the remainder of the revolution of the drum since the end of record
13 character also turns off write complete flip-flop 154 which blocks status
14 empty pulses from reaching head delay and single shot 207, delays 208
15 and 219, and flip-flop 221. Upon completion of the revolution, detection
16 of the region start character turns on write complete flip-flop 154 so as
17 to reset the system and again allow pulses to reach block length flip-
18 flop 221.

19 **WRITE OPERATION**

20 Referring to Fig. 3B, the example illustrated is the
21 writing of record no. 8 into the region after record no. 2 has been
22 purged and determining and applying the number 4 as the chain number.

23 Referring additionally to Fig. 1, the program 32 of the
24 CPU 10 reaches an instruction commanding that record no. 8 be written
25 in the cyclic file 12. To accomplish this, the CPU selects the desired
26 region by appropriate signals on track select line 28, which is inter-
27 preted by file control unit 11 to select, via control line 29, the desired
28 track. The CPU then transmits a signal on command write line 41 and
29 transmits the data comprising record no. 8 on write data cable 40.

30 Referring additionally to Fig. 4, the signal on line 41

operates the switching means to throw switches 130-137 to the "W" position. Record no. 8 appearing on cable 40 is read into and stored by input buffer register 120.

Then, nothing of importance happens until the region start character is read by read head 101 and read amplifier 105 and deserialized by deserializer 110. Upon the completion of deserialization, at the end of the character time, the parallel data is transmitted to single character register 112. The register stores the data for one character time during which it transmits the data on line 140. The character is detected by detect region start circuit 142 which thereby transmits a signal on line 150 for the duration of the character time that the character is received from single character register 112.

This signal on line 150 resets block counter 151 to zero, turns write complete flip-flop 154 on, and is transmitted by OR circuit 152 to turn on block counter flip-flop 156. The output of write complete flip-flop 154 activates one input of AND circuit 158 so that subsequent outputs of detect status empty circuit 172 will be gated therethrough. The output of block counter flip-flop 156 provides one input to AND circuit 157 so that the subsequent block start signal will be gated to the COUNT input of block counter 151. Thus, the system is reset and in condition for writing record no. 8 into the first available empty blocks.

The first block to be detected is block no. 1, which already has record no. 1 stored therein. The block start character of block no. 1 is read, serialized, and stored in single character register 112 for the subsequent character time. The character is detected by detect block start circuit 143 and an output signal transmitted therefrom on line 160. The positive-going portion of the output is received by, although it has no effect upon, status flip-flop 161 or one character single shot 162. The signal on line 160, however, is gated by AND

1 circuit 157, as previously stated, to the COUNT input of block counter
2 151. The first stage of the lowest order counter is then activated so as
3 to provide the coded signal representative of number 1 to the internal
4 gate circuits.

5 At the conclusion of the block start signal on line 160, the
6 negative-going portion of the signal turns on status flip-flop 161 and
7 operates one character single shot 162. The output of status flip-flop
8 161 operates gate 144 to transmit therethrough the following character,
9 which is the status character.

10 Immediately thereafter the status character is transmitted
11 on cable 140, through gate 144, to detect status full circuit 171 and to
12 detect status empty circuit 172. Since, as shown in Fig. 3B, record
13 no. 1 is already stored in block no. 1, detect status full circuit 171
14 provides an output while detect status empty circuit 172 does not.
15 Thus, since switch 136 is in the write position, no signal appears on
16 line 190 and no input is applied to the SET OFF input of block counter
17 flip-flop 156.

18 At the conclusion of the transmission of the status character
19 by single character register 112, one character single shot 162 trans-
20 mits an output on line 164 thereby turning off status flip-flop 161.
21 This prevents further transmission of characters by gate 144.

22 In summary, the region start character has reset the
23 system and the block start character of block no. 1 was counted by
24 block counter 151 and the status character has been detected. Since
25 the status character indicated block no. 1 was full, no chain number
26 was established by transmission of the count from the block counter
27 and no data was written into the block.

28 Since block nos. 2 and 3 are also full, the system operates
29 similarly for each of the blocks so that block counter 151 counts each
30 one to thereby store the count of three, and no data is written in any
31 of the blocks.

Block no. 4, which has been purged together with block 300, now begins to appear under read head 101. Its block start character is read, deserialized and stored in single character register 112 for the subsequent character time. Circuit 143 detects the block start character and provides an output on line 160, which is transmitted by AND circuit 157 to the COUNT input of block counter 151. The counter responds by advancing one step so as to provide the coded signal representative of number 4 to the internal gate circuits.

10 The negative-going portion of the block start signal on line 160 turns on status flip-flop 161 and operates one character single shot 162. Again, the output of the status flip-flop operates gate 144 to transmit therethrough the immediately following status character. The status character is transmitted via cable 140 and gate 144 to circuits 171 and 172. As shown in Fig. 38, block no. 4 has been purged; therefore, detect status empty circuit 172 provides an output which is transmitted by AND circuit 158 and switch 136 onto line 190.

20 The signal on line 190 is transmitted by switch 131 to operate set status full circuit 200, and also transmitted through OR circuit 201 to the input of head delay and single shot 207. Set status full circuit 200 responds by transmitting parallel data representing the status full character via cable 202 and OR circuit 203 to the input to single character register 204, thereby setting the flip-flops within the register to correspond to the status full character. The delay portion of head delay and single shot circuit 207 delays the input thereto the amount of time required for the status character position to begin to appear under write head 102. At this time the single shot is operated and provides a signal to one character delay 208 and via the command readout line 205 to single character register 204. This gates the AND circuits therein to gate the outputs of the flip-flop onto cable 206. This status full character is transmitted by OR circuit 122 to serializer 111.

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1 which serializes the character and transmits the data to write amplifier
2 106 which causes write head 102 to write the character in serial fashion
3 in the status character position. Thus, the status of the block is
4 changed from empty to full.

5 The negative-going portion of the signal on line 205 then
6 resets the flip-flops of single character register 204 to their off state.

7 A signal appearing on line 190 also is transmitted to the
8 SET OFF input of block counter flip-flop 156 thereby turning the flip-
9 flop off. This removes the gating input from AND circuit 157 and will
10 block the transmission of any further block start pulses therethrough,
11 thereby preventing further incrementing of block counter 151. Thus,
12 the number 4 is now stored in the counter.

13 At the end of the transmission of the status character by
14 single character register 112, one character single shot returns to its
15 normally on condition, thereby turning off status flip-flop 161 so as to
16 close gate 144 and prevent the transmission of data to circuits 171 and
17 172.

18 Immediately after the status full character has been written
19 into the status area of block no. 4, one character delay circuit 208
20 provides an output via switch 130 and line 214 to the GATE input of block
21 counter 151 and to four character delay 215. The positive-going portion
22 of the signal at the GATE input to the block counter operates the internal
23 output clock and gating circuits so as to sequentially transmit the
24 parallel characters comprising the chain number via cable 210, switch
25 133 and OR circuit 122 to serializer 111. The serializer changes the
26 data to serial form and transmits it to write amplifier 106 which writes
27 the data into the chain number area of block no. 4. As previously
28 described, the chain number is the numeral "4" representing block no. 4
29 which is the first block in which data of record no. 8 is to be written.

30 Immediately after the chain number has been written, four

1 character delay 215 provides an output via OR circuit 220 to turn on
2 block length flip-flop 221. The output of the flip-flop is supplied to
3 one input of AND circuit 223 and is transmitted via switch 134 to the
4 READOUT input 121 of input buffer register, 120. This gates the output
5 of the character clock of the file control unit to the register thereby
6 operating the register such that it transmits one character of data for
7 each character time through OR circuit 122 to serializer 111 which
8 causes the data to be written in the data area of block no. 4.

9 The character clock is also connected to the second input
10 of AND circuit 223. Since flip-flop 221 is on, the character clock
11 pulses are gated through the AND circuit to the COUNT input of block
12 length counter 224. The counter is incremented by each character
13 clock pulse which represents one character as written in the data area
14 of the block. When the block length counter reaches the count repre-
15 senting the number of characters capable of being stored in the data
16 area, it provides an output to OR circuit 225 for one character time
17 and then automatically resets. This output is transmitted by OR
18 circuit 225 to turn off block length flip-flop 221. This removes the
19 one input to AND circuit 223 preventing the transmission of any further
20 clock pulses to the counter and simultaneously turns off the input buffer
21 register 120 to stop the transmission of data to serializer 111. Thus,
22 the block length counter and block length flip-flop control the amount
23 of data written from the input buffer register into the data area of
24 block no. 4 so that the data written therein corresponds exactly to the
25 space available.

26 In summary, the system bypasses block nos. 1, 2 and 3
27 since they were indicated as being full and the block counter kept
28 track of the number of blocks so detected. Block no. 4 was the first
29 available block so its status was changed from empty to full, its
30 number was stored in block counter 151 as the chain number, the chain

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1 number written in the chain number area of block no. 4, and the first
2 portion of data of record no. 8 written into the data area of block no. 4.
3 The block start character of block no. 5 is detected by
4 circuit 143 and the output therefrom is blocked from block counter 151
5 by AND circuit 157 because block counter flip-flop 156 remains off.
6 Thus, the counter remains set at number 4.
7 The negative-going portion of the block start signal operates
8 status flip-flop 161 and one character single shot 162 so as to open gate
9 144 for one character time period.
10 The status character is then transmitted through gate 144
11 to circuits 171 and 172. Since the character indicates that the block is
12 empty, circuit 172 provides an output through AND circuit 158 to set
13 status full circuit 200, OR circuit 201 and block counter flip-flop 156.
14 The signal has no effect on the block counter flip-flop since the counter
15 is already off. As before, the signal received by set status full circuit
16 200 and OR circuit 201 is utilized by circuit 200, head delay and single
17 shot 207, and single character register 204 to write the status full
18 character into the status area of block no. 5 when it appears under
19 write head 202.
20 After the status character has been written, one character
21 delay 208 provides an output which operates the GATE input of the block
22 counter so that it provides, as before, the chain number on its cable 210,
23 which is serialized by serializer 111 and written into the chain number
24 area of record no. 5. Thus, the chain number "4" written into the
25 chain number area of record no. 5 is the same as that written into the
26 chain number area of record no. 4.
27 After the chain number has been written, four character
28 delay 215 provides an output via OR circuit 220 to block length flip-
29 flop 221, which turns on and operates input buffer register 120 to begin
30 transmitting data to be written in the data area of record no. 5. The

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1 block length flip-flop also operates AND circuit 223 to gate character
2 clock pulses to the block length counter which again turns off block
3 length flip-flop 221 when the maximum number of characters have been
4 written into record no. 5. This turns off the block length flip-flop which
5 stops the operation of input buffer register 120.

6 The block start character for record no. 6 is detected by
7 circuit 143 and the output therefrom is again blocked from reaching
8 block counter 151 by AND gate 157 since block counter flip-flop 156
9 remains off. The negative-going portion of the output of circuit 143
10 again operates status flip-flop 161 and one character single shot 162 to
11 gate the status character to circuits 171 and 172.

12 The status character for record no. 6, however, indicates
13 the block is full; therefore, circuit 171 provides an output to the open
14 side of switch 136 and no output is provided by circuit 172. As a result,
15 nothing further happens to the system except that status flip-flop 161
16 is turned off by one character single shot 162 thereby closing gate 144.

17 Thus, block no. 6, being full, is skipped over and has no
18 effect on the system. Similarly, since blocks 7-21 are also indicated
19 as being full, they too are skipped over and have no effect on the system.

20 The block start character pulse for block no. 22 is prevented
21 from reaching block counter 151 due to block counter flip-flop 156 being
22 off and thereby closing AND circuit 157. The character does cause
23 status flip-flop 161 to open gate 144 for the subsequent character time
24 period during which the status character is gated to circuits 171 and 172.

25 Since block no. 22 is empty, circuit 172 will provide an
26 output on line 190 to operate set status full circuit 200 and the associated
27 circuitry to write a status full character into the status area of block
28 no. 22.

29 Again, the output of one character delay 205 operates the
30 block counter 151 to transmit data to serialiser 111 for writing the

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chain number in the chain number area of block no. 22. Subsequently, four character delay 215 turns on block length flip-flop 221 so as to control input buffer register 120 to transmit more data of record no. 8 to the data area of block no. 22 until terminated by block length counter 224.

Finally, the block start character of block no. 23 is detected by detect block start circuit 143 which provides an output, the negative-going portion of which operates status flip-flop 161 to open gate 144.

10 The status character is then transmitted through gate 144 to circuits 171 and 172. Again, the status is empty so that circuit 172 provides an output on line 190. This output operates set status full circuit 200 and the associated circuitry to write the status full character into the status area of block no. 23. Then, one character delay 208 provides an output operating block counter 151 to transmit the chain number "4" to serializer 111 so that it is written in the chain number area of the block. Next, four character delay 215 turns on block length flip-flop 221 so that it operates input buffer register 120, which transmits the remaining data of record no. 8 to serializer 111 to be written in the data area of the block.

20 However, before block length counter 224 can count the number of characters for the entire data area of the block, the input buffer register transmits the end of record character which indicates the actual end of record no. 8. This character is transmitted to and serialized by serializer 111 and written at the end of the data of record no. 8. The character is also transmitted through OR circuit 230 to detect end of record circuit 231. In response thereto, the circuit provides an output on line 182 which is transmitted through OR circuit 225 to turn off block length flip-flop 221. This immediately terminates the operation of the input buffer register 120 without waiting for block length counter 224 to reach its complete count. The signal on line 182 also

1 resets block length counter 224 to zero. Thus, detection of the end of
2 record character operates to end transmission of data to serialiser 111
3 so that no data from a subsequent record, if stored in the register, is
4 written in a block occupied by another record.

5 The output of detect end of record circuit 231 is also applied
6 to turn off write complete flip-flop 154 which prevents output signals
7 from detect status empty circuit 172 from being transmitted by AND
8 circuit 158. This prevents further operation of the system until the
9 next region start character is detected.

10 In summary, the disclosed system has accepted data from
11 the CPU 10 and stored this data in an input buffer register 120. The
12 system then examined the status of each block detected while keeping
13 track of the number of blocks so detected until the first available empty
14 block was indicated by its status character. Then, the count in the
15 block counter after detecting this block remained stored in block counter
16 151 as the chain number. The system changed the status character in
17 block no. 4 from empty to full, wrote chain no. "4" in the chain number
18 area of the block, and wrote the first portion of data of record no. 8
19 into the data area of block no. 4. Then, the system detected that block
20 no. 5 was empty and changed its status character from empty to full,
21 wrote the chain number in its chain number area, and wrote more data
22 of record no. 8 in its data area. Blocks 6-21 were all indicated as full
23 so were skipped by the system. Block no. 22 was detected as being
24 empty and its status character changed, the chain number inserted,
25 and more data written therein. Finally, block no. 23 was detected as
26 being empty, its status character changed, the chain number written in
27 the chain number area, and the last of the data of record no. 8 written
28 in the data area thereof, including the end of record character. Upon
29 detection of this end of record character, input buffer register 120 was
30 stopped from transmitting more data and write complete flip-flop 154

1 turned off to prevent further operation of the system upon detection of
2 states empty characters until a region start character could reset the
3 system.

4 **READ CIRCUITRY**

5 As described with respect to Figs. 1-3, the CPU 10 reads
6 data from cyclic file 12 by transmitting an appropriate coded signal
7 over track select cable 15 to select the desired region and then by
8 transmitting a signal on command read line 43 to file control unit 11.
9 The file control unit transmits signals on control line 16 to select the
10 desired track and begin receipt of data from the cyclic file on read
11 cable 30. The file control unit then transmits the data from the data
12 area 25 of the first block of each record to the CPU over line 31. The
13 program 32 of the CPU selects the desired data by continually com-
14 paring the incoming data to the designation of desired data. If, as each
15 such block is being read, no comparison is made, the program causes
16 the CPU to supply a signal on reject line 33 to the file control unit.
17 The file control unit will therefore continue transmitting data from the
18 first block of each record to the CPU until a comparison is made and
19 no signal is transmitted on reject line 33. The system then automatic-
20 ally transmits only the data comprising the remainder of the selected
21 record on cable 31 to the CPU.

22 Referring now to Fig. 4, the command read signal on line
23 43 operates a latch circuit (not shown) which in turn operates switches
24 130-137 to the "R" or "Read" position. The latch remains on until
25 such time as the CPU transmits a command write signal.

26 As previously stated, the data on track 103 of drum 100 of
27 the cyclic file is continually read by read head 101 and read amplifier
28 105, and the data is converted into parallel characters by deserialiser
29 110 and transmitted to single character register 112. The register
30 stores the data representing one character for the duration of a single

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1 character time and transmits the data on cable 140 during this time.
2 Detect region start circuit 142 is connected to cable 140
3 and detects the region start character whenever it appears thereon.
4 As previously explained, this circuit then provides an output on line 150
5 which resets block counter 151 to zero and is transmitted through OR
6 circuit 152 to turn on block counter flip-flop 156.

7 As will be explained hereinafter, the functions of block
8 counter 151 and block counter flip-flop 156 are to count the number of
9 blocks detected until the first block having the selected data is detected
10 and no reject signal is transmitted from the CPU. The resultant count
11 remains stored in the block counter and comprises the chain number
12 for the record being read from storage. Thus, when the region start
13 pulse resets block counter 151 to zero and turns on the block counter
14 flip-flop 156, the system is set to begin counting the block start
15 characters as transmitted through AND circuit 157 to the COUNT input
16 of the block counter. As will be explained hereinafter, block counter
17 flip-flop 156 is connected to gate the block start signals until no further
18 reject signals are received, indicating the desired record is being
19 read. Thus, the block counter will contain the number of the block in
20 which the beginning of the desired record is located.

21 As previously described, detect block start circuit 143
22 provides an output upon detection of a block start character. This
23 output is transmitted on line 160 to be gated through AND circuit 157,
24 so long as block counter flip-flop 156 is on, to the COUNT input of block
25 counter 151. The negative-going portion of the block start pulse operates
26 status flip-flop 161 and one character single shot 162 to open gate 144
27 for one character time immediately following each block start character.
28 This gates the status character to detect status full circuit 171 and to
29 detect status empty circuit 172. Switch 136 is in the "R" position so a
30 status empty character produces no effect and detection of a status full

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1 character by circuit 171 produces an output via line 180 and switch 136
2 to line 190.

3 Line 190 is connected to, internally, the SET OFF input of
4 block counter flip-flop 156 and to one character delay 191.

5 Since any full block may contain the desired data, the output
6 of detect status full circuit 171, appearing on line 190, is used to turn
7 off block counter flip-flop 156. This prevents further block start pulses
8 from being gated to block counter 151 unless a reject signal is received
9 from the CPU on line 33. The reject signal indicates that the data read
10 was not the desired data; therefore, the reject signal is transmitted by
11 OR circuit 152 to the SET ON input of block counter flip-flop 156 to turn
12 the flip-flop on. This allows the following block start signal to be
13 transmitted to the COUNT input of block counter 151 to designate the
14 data then being transmitted to the CPU over line 31.

15 The CPU indicates that the data being received over line 31
16 is the desired data by not transmitting a reject signal on line 33. This
17 leaves block counter flip-flop 156 off, blocking AND circuit 157 from
18 transmitting further block start pulses to block counter 151, thereby
19 preventing further incrementing of the counter. The counter, therefore,
20 contains as its count a number designating the block having the beginning
21 of the desired record contained therein. This number is then the chain
22 number designating the following blocks which contain the remainder of
23 the selected record.

24 As previously mentioned, line 190 from detect status full
25 circuit 171 is connected to one character delay 191. The one character
26 delay is identical to one character delay 208, previously described,
27 and provides at its output a signal identical to that provided at its input
28 one character time later. The one character delay is connected to the
29 SET ON input of chain number flip-flop 240 and to the "R" contact of
30 switch 130.

1 Chain number flip-flop 240 comprises a conventional flip-
2 flop circuit identical in construction to that of block counter flip-flop
3 156. The output of the flip-flop is connected to the control input of gate
4 circuit 241. The flip-flop thereby controls the gating of data from single
5 character register 112 via gate circuit 241 and cable 242 to compare
6 block count and chain number circuit 211 to compare chain number and
7 purge register circuit 217 and to gate circuit 243. One character delay
8 191 is connected via switch 130 and line 214 to the GATE input of block
9 counter 151 and to four character delay 215. The four character delay,
10 previously described, provides an output identical to that received from
11 line 214 on its output four character times later. The output of the four
12 character delay is applied to the SET OFF input to chain number flip-
13 flop 240.

14 Therefore, a status full pulse is supplied on line 190 by
15 circuit 171 and is delayed one character time by one character delay 191.
16 Upon completion of transmission of the status full character by single
17 character register 112, delay 191 provides an output which simultaneously
18 turns on chain number flip-flop 240 and operates the GATE input of block
19 counter 151. Thus, data from cable 140, comprising the chain number
20 of the block being read, is transmitted through gate 241 due to the
21 operation of chain number flip-flop 240 simultaneously with the trans-
22 mission of the count of block counter 151 onto cable 210 due to the
23 operation of the stepping means and gating circuits of the block counter.
24 This data is therefore transmitted simultaneously character-by-character
25 to compare block count and chain number circuit 211.

26 The stepping circuit of block counter 151 automatically
27 transmits the four characters stored therein and then returns to the
28 rest position. Four character delay 215 provides at its output the pulse
29 received from one character delay 191 four character times later. This
30 output turns off chain number flip-flop 240. Therefore, the output of the

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1 character delay 191 turns on chain number flip-flop 240 and operates
2 four character delay 215 which turns off the chain number flip-flop
3 four character times later. This allows the gating of data from each
4 detected full block representing only the chain number thereof. Thus,
5 only the four characters comprising the block count and the four
6 characters comprising the chain number are compared a character at
7 a time by compare block count and chain number circuit 211.

8 Circuit 211 comprises a plurality of logical comparison
9 circuits, each having two inputs connected to corresponding lines and
10 cables 210 and 242. The circuits are arranged such that, upon receipt
11 of data from either cable, the comparison circuits provide an output if
12 the inputs on each of the corresponding lines are identical. The com-
13 parison circuits are ANDed together such that all of the comparison
14 circuits must indicate that a comparison is made in order for there to
15 be an output from the AND circuit. The AND circuit is connected to a
16 four stage binary counter having an output at the fourth stage and having
17 a fifth rest stage. If the first set of characters received from block
18 counter 151 and gate 241 correspond, the AND circuit will provide an
19 output and step the binary counter to the first stage from the rest stage.
20 If the three following characters also compare, the AND circuit will
21 provide three pulses to step the counter to the fourth stage, providing
22 an output therefrom. If four comparisons are not made, the binary
23 counter does not reach the fourth stage. Therefore, there is no output.

24 A gate circuit is connected to the output of the fourth stage.
25 A timing means contained in circuit 211 is connected to the control
26 input of the gate and to the rest stage of the computer. The timing
27 means automatically turns on the gate four character times after the
28 beginning of receipt of data from block counter 151 or gate 241 and also
29 turns off that gate and resets the binary counter to the rest stage five
30 character times after the beginning of receipt of data from block counter

1 151 or gate 241.

2 Therefore, if the block count received from circuit 151 is
3 identical to the chain number received from gate 241, circuit 211
4 produces an output signal immediately after the end of the chain number
5 which lasts for one character time. The binary counter is then auto-
6 matically turned off and resumes the rest position.

7 The output of circuit 211 is directed via switch 135, which
8 is in the read position, to OR circuit 220.

9 OR circuit 220, block length flip-flop 221, block length
10 counter 224 and the circuitry associated therewith have been previously
11 described with respect to the write function. When circuit 211 indicates
12 that the chain number and block count agree, the pulse appearing
13 immediately after the chain number therefrom is transmitted through
14 OR circuit 220 to turn on block length flip-flop 221. This produces an
15 output on line 222, which is transmitted to AND circuit 223. AND
16 circuit 223 responds by gating character clock pulses therethrough to
17 the COUNT input of block length counter 224. Upon reaching the count
18 designating the length of the data area of a block, counter 224 produces
19 an output which is transmitted via OR circuit 225 to turn off block
20 length flip-flop 221. Thus, an output appears on line 222 for the length
21 of the data area of the block in which the block count and chain number
22 have agreed.

23 Since the block count and chain number agree for each
24 block which is the first block of a record, the complete data for each
25 such block is gated until reject signals are no longer received on line
26 33. Then, the block count remains locked on the chain number of the
27 desired record so that only those records having the chain number of
28 the desired record will cause circuit 211 to produce a signal thereby
29 activating the block length flip-flop 221.

30 The output of the block length flip-flop is connected via

1 switch 234, which is in the read position, to the control input of gate
2 circuit 141. This gate controls the transmission of data from single
3 character register 112, via cable 244, to output buffer register 245.
4 Thus, whenever an output is provided by compare circuit 211, the
5 block length circuitry provides a signal on line 222 which opens gate 141
6 for the length of time required to transmit therethrough all of the data
7 contained in the data area of a block.

8 Output buffer register 245 is a register for storing
9 characters in parallel and is identical in construction to input buffer
10 register 120. In some configurations it may be desirable to have a
11 readout input to allow the CPU to control the reading of data from the
12 register. However, in the illustrative embodiment, the register stores
13 a block of data as received from single character register 112, stores
14 that data and delivers the data, parallel by bit and serial by character,
15 over data out cable 31 to the CPU using the timing of the CPU.

16 The output of gate 141 is also connected through OR cir-
17 cuit 230 to detect end of record circuit 231 which has been previously
18 described. Thus, all of the data in the data area of each block trans-
19 mitted to output buffer register 245 is also transmitted through OR
20 circuit 230 to circuit 231.

21 At some point, while the data of a record is being read, an
22 end of record character of that record will appear. This end of record
23 character is detected by detect end of record circuit 231 which responds
24 by providing an output signal on line 182 which is transmitted through
25 OR circuit 225 to turn off block length flip-flop 221. This immediately
26 closes gate 141 without waiting for the block length counter 224 to
27 reach its ultimate count. This thereby terminates the transmission
28 of data upon detection of an end of record character rather than waiting
29 for the end of the data area to appear.

30 The output line 182 from detect end of record circuit 231 is

1 also connected to the RESET input of block length counter 224 to reset
2 the counter to zero.

3 The system thus automatically terminates transmission of
4 data after receipt of an end of record character and resets the counter
5 224 to zero, but does not prevent further operation of the system.
6 This is provided in view of the fact that some records may be less than
7 one block in length and therefore, the block count and chain number
8 would agree for this record if the desired record had not yet been
9 detected. Thus, even though an end of record character for this block
10 is detected, it remains necessary to search additional blocks to locate
11 the desired record.

12 It is necessary to end the transmission of data immediately
13 upon receipt of an end of record character because the system provides
14 no means for erasure. Data from previously recorded records not
15 written over by data from the present record could possibly get through
16 and cause erroneous results by the CPU if it were allowed to be trans-
17 mitted thereto. Therefore, the end of record character is significant
18 in promoting the reliability of the system.

19 **READ OPERATION**

20 Referring to Fig. 3B, the example illustrated is the reading
21 of record no. 8 from a selected region.

22 Referring additionally to Fig. 1, the program 32 of the CPU
23 10 reaches an instruction commanding that a record from a selected
24 region of cyclic file 12 having specific identifying data be read. To
25 accomplish this, the CPU selects the desired region by appropriate
26 signals on track select line 28, which is interpreted by file control unit
27 11 to select, via control line 29, the desired track. The CPU then
28 transmits a signal on command read line 43. The CPU may then go
29 about other business while standing by to compare data appearing on data
30 out cable 31 with the specified designating data.

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1 Referring additionally to Fig. 4, the signal on line 43
2 operates the switching means to throw switches 130-137 to the "R"
3 or "Read" position. Then, nothing of importance happens until the
4 region start character is read by read head 101 and read amplifier 105
5 and deserialized by deserializer 110. Upon completion of deserialization,
6 at the end of the character time, the parallel data is transmitted to
7 single character register 112. The register stores the data for one
8 character time during which it transmits the data on cable 140. The
9 region start character is detected by detect region start circuit 142,
10 which thereby transmits the signal on line 150 for the duration of the
11 character time that the character is received from single character
12 register 112.

13 This signal on line 150 resets block counter 151 to zero
14 and is transmitted by OR circuit 152 to turn on block counter flip-flop
15 156. The output of the block counter flip-flop provides one input to
16 AND circuit 157 so that the subsequent block start signal will be gated
17 to the COUNT input of block counter 151. Thus, the system is reset
18 and in condition for reading the data from the first block of each record
19 to the CPU as long as reject signals are received on line 33.

20 The first block to be detected is block no. 1, which has
21 record no. 1 stored therein. The block start character for block no. 1
22 is read, deserialized and stored in single character register 112 for
23 the subsequent character time. This character is detected by detect
24 block start circuit 143 and an output signal transmitted therefrom on
25 line 160. The positive-going portion of the output is gated by AND
26 circuit 157, as previously stated, to the COUNT input of block counter
27 151. This increments the counter by one so that the first stage of the
28 lowest order counter is then activated. This provides a coded signal
29 representative of no. 1 to the internal gate circuits.

30 At the conclusion of the block start signal on line 160, the

1 negative-going portion of the signal turns on status flip-flop 161 and
2 operates one character single shot 162. The output of status flip-flop
3 161 operates gate 144 to transmit therethrough the immediately following
4 character, which is the status character. One character time later,
5 single shot 162 turns off status flip-flop 161 and blocks gate 144.

6 The status character is transmitted by single character
7 register 112 through gate 144 to detect status full circuit 171 and to
8 detect status empty circuit 172. Since, as shown in Fig. 3B, record
9 no. 1 is stored in block no. 1, detect status full circuit 171 provides an
10 output while detect status empty circuit 172 does not. Thus, since
11 switch 136 is in the read position, the output of circuit 171 appears on
12 line 190 to turn off block counter flip-flop 156 and to operate one
13 character delay 191. Turning off block counter flip-flop 156 prevents
14 AND circuit 157 from transmitting further block start pulses to block
15 counter 151 while the block counter flip-flop remains off. This prevents
16 further incrementing of the counter so that it contains as its count a
17 number 1 which designates block no. 1 which has the beginning of
18 record no. 1 contained therein. If record no. 1 is the desired record,
19 the count contained in the counter will be utilized to designate the chain
20 number for additional blocks containing that record.

21 Immediately after the transmission of the block start
22 character from single character register 112, one character delay 191
23 provides an output to turn on chain number flip-flop 240, to operate,
24 via switch 130, the GATE input of block counter 151, and to operate
25 four character delay 215. When turned on, chain number flip-flop 240
26 operates gate 241 to gate therethrough data appearing at the output
27 cable 140 of single character register 112. This data comprises the
28 chain-number of block no. 1, which is thereby gated on line 232 to one
29 input of compare block count and chain number circuit 211. Simultane-
30 ously, the output of one character delay 191 operates the stepping circuit

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1 and internal gates of block counter 151 to transmit, via cable 210, the
2 count stored therein to the other input of compare circuit 211. After
3 the complete chain number has been transmitted on line 232 to the
4 compare circuit, four character delay 215 provides an output on line
5 216 to turn off chain number flip-flop 240. This terminates further
6 transmission through gate 241.

7 As shown in Fig. 3B, the block no. "1" and the chain no.
8 "1" are the same. Thus, a comparison is made by compare circuit 211
9 and an output provided for one character time immediately after the
10 comparison. This output is transmitted through switch 135 and OR
11 circuit 220 to turn on block length flip-flop 221. The flip-flop provides
12 an output on line 222 which operates gate 223 to gate character clock
13 pulses to block length counter 224. The counter counts the character
14 pulses until sufficient pulses have been counted to indicate the end of
15 a data area. The counter then provides an output which is transmitted
16 through OR circuit 225 to turn off block length flip-flop 221. This
17 terminates the output pulse on line 222.

18 Line 222 is connected through switch 134 to gate circuit 141.
19 The pulse on line 222 appears for the duration of the data area of block
20 no. 1 and gate 141 responds by gating the data from single character
21 register 112 to cable 244. Cable 244 is connected to output buffer
22 register 245 and transmits the data thereto, which in turn retransmits
23 the data on data out cable 40 to the CPU at CPU timing.

24 The CPU detects this data and, since record no. 8 is
25 desired, the program 32 rejects the data from record no. 1 by providing
26 a reject signal on line 33. This signal is transmitted by OR circuit 152
27 to turn on block counter flip-flop 156, which operates AND circuit 157
28 to gate the subsequent block start character.

29 The block start character for block no. 2 is then detected
30 by circuit 143 and gated by AND circuit 157 to block counter 151. This

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1 increments the block counter so that it now contains the number "2".

2 The negative-going portion of the block start signal turns on status

3 flip-flop 161 and operates one character single shot 162 to gate the

4 status character through gate 144.

5 Again, block no. 2 is full so circuit 171 provides an output

6 on line 190 which turns off block counter flip-flop 156, blocking AND

7 circuit 157 and which operates one character delay 191.

8 One character time later, delay 191 turns on chain number

9 flip-flop 240 operating gate 241 and is transmitted via switch 130 to

10 operate the GATE input of block counter 151. Thus, the chain number

11 of block no. 2 is transmitted through gate 241 simultaneously with the

12 transmission of the count from block counter 151 to compare circuit 211.

13 In this case, counter 151 provides the number "2" and the

14 chain number provided through gate 241 is the number "1", so no com-

15 parison is made. Thus, circuit 211 does not provide an output and the

16 block length circuitry is not operated thereby blocking gate 141 from

17 transmitting data therethrough. At the end of the chain number, four

18 character delay 215 turns off chain number flip-flop 240 thereby blocking

19 gate 241. Since no data is received by the CPU, it again transmits a

20 signal on reject line 33, turning on the block counter flip-flop 156.

21 Block no. 3 is treated similarly, incrementing the block

22 counter 151 to the number "3" and preventing the transmission of data.

23 Again, the CPU sends a reject signal on line 33 turning on flip-flop 156.

24 Referring to block no. 4, the block start character is

25 detected by circuit 143 and the block start signal is counted by block

26 counter 151 thereby providing the number "4". The negative-going

27 portion of the block start signal operates the status flip-flop 161 and

28 single shot 162 to operate gate 144 during the status character time.

29 The status character is then gated therethrough and, since the block is

30 full, detect status full circuit 171 provides an output on line 190. This

1 output turns off block counter flip-flop 156 and operates one character
2 delay 191. Again, the delay operates block counter 151 and chain
3 number flip-flop 240 to gate the chain number and block count to com-
4 parison circuit 211. Now, the block number is number "4" and the
5 chain number is also number "4", so the compare circuit 211 provides
6 an output which turns on block length flip-flop 221. The block length
7 circuitry then operates to open gate 141 for the time comprising the
8 data area of block no. 4, thereby gating the data of block no. 4 to output
9 buffer register 245. The buffer register retransmits the data to the
10 CPU on cable 31 and the program 32 of the CPU detects that the selection
11 requirements are satisfied thereby.

12 Thus, the CPU does not transmit a reject signal on line 33.
13 Block counter flip-flop 156, therefore, remains off and prevents any
14 further block start characters from reaching block counter 151 through
15 AND circuit 157. The block counter, therefore, is locked on the
16 number "4" which is the chain number of the desired record.

17 Next, the block start character for block no. 5 is detected
18 by circuit 143. The resultant signal on line 160 is blocked by AND
19 circuit 157 since block counter flip-flop 156 is off. Thus, block counter
20 151 remains locked at the number "4".

21 The negative-going portion of the block start signal operates
22 status flip-flop 161 and one character single shot 162 to open gate 144
23 for the status character. The status character, again indicating full,
24 causes circuit 171 to produce an output on line 190. This output has
25 no effect on the block counter flip-flop 156, but operates one character
26 delay 191. At the end of the status character, delay 191 operates the
27 chain number flip-flop 240 and block counter 151 so that the chain
28 number of block no. 5 is gated through gate 241 to compare circuit 211
29 and block counter 151 transmits the stored number "4" to the compare
30 circuit. Again, the chain number and output of block counter 151 are

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1 Identical, so circuit 211 turns on the block length circuitry. The block
2 length circuitry operates gate 141 to allow all of the data of block no. 5
3 to be transmitted to output buffer register 245, which retransmits the
4 data to the CPU.

5 The block start character for block no. 6 has no effect on
6 block counter 151. The signal also operates the status flip-flop 161 and
7 associated circuitry to open gate 144 and allow the status character
8 therethrough. Again, since block no. 6 is indicated as being full, cir-
9 cuit 171 provides an output on line 190 which has no effect on block
10 counter flip-flop 156, but which operates one character delay 191.
11 Again, the delay operates chain number flip-flop 240, the GATE input
12 to block counter 151 and four character delay 215 to gate the number
13 "4" representing the block count from counter 151 and simultaneously
14 gating the chain number "6" from the single character register 112 to
15 compare circuit 211. Since the numbers are different, no comparison
16 is made and the block length circuitry is not operated, preventing the
17 transmission of data to the CPU.

18 Blocks 7-21 are all full, but all have chain numbers different
19 than the number "4" contained in block counter 151. Therefore, com-
20 pare circuit 211 never makes a comparison and no data is transmitted
21 to the CPU.

22 Upon reaching block no. 22, the positive-going portion of
23 the output of circuit 143 has no effect since AND circuit 157 remains
24 blocked by clock counter flip-flop 156. The negative-going portion of
25 the signal operates the status flip-flop 161 to open gate 144 which is
26 closed one character time later by the operation of single shot 162.
27 The status character gated therethrough indicates the block is full and
28 causes circuit 171 to provide an output. The output is directed over
29 line 190 to operate one character delay 191. The output has no effect
30 on block counter flip-flop 156, since it is already off.

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1 The output of delay 191 again operates block counter 151
2 and, via chain number flip-flop 240, operates gate 241 to transmit
3 the chain number "4" from single character register 140 and the block
4 count number "4" from counter 151 to compare circuit 211. A com-
5 parison is made and the output therefrom operates the block length
6 circuitry to open gate 141 to allow the transmission of data from block
7 no. 8 therethrough. The data is received and retransmitted by output
8 buffer register 245 to CPU 10.

9 Block no. 23 is similarly treated in that the chain number
10 agrees with the block count so comparison circuit 211 provides an
11 output to turn on block length flip-flop 221. This again gates character
12 clock pulses through AND circuit 223 to block length counter 224 and
13 also opens gate 141 to transmit data from single character register 112
14 to output buffer register 245.

15 However, an end of record character is contained in the
16 data area of block no. 23 and is transmitted by single character
17 register 112 before block length counter 224 reaches its ultimate count.
18 Therefore, the end of record character, as transmitted on cable 244,
19 is detected by detect end of record circuit 231. The circuit then provides
20 an output on line 182 which is transmitted through OR circuit 225 to
21 turn off block length flip-flop 221 and which resets the block length
22 counter to zero. When turned off, the block length flip-flop removes the
23 gating signal from gate 141 thereby preventing further transmission of
24 data therethrough. In this manner, no data beyond the end of record
25 character is transmitted to the output buffer register. Thus, after the
26 desired record has been selected, the system transmits to the CPU
27 only that data comprising the data of record no. 8 including the end of
28 record character. No remaining unerased data of block no. 23 is
29 transmitted. The reliability of this system is thus assured.

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1 PURGE CIRCUITRY

2 As described with respect to Figs. 1-3, the CPU enters
3 the purge mode by transmitting signals on command purge line 34 and
4 command read line 43. Thus, the purging function utilizes the reading
5 function to read the first block of each record until the selected block
6 is detected. When the program 12 detects the selected record, no
7 reject signal is transmitted on line 33 in accordance with the read
8 function, and, in addition, a command purge signal of two character
9 length duration is then transmitted on line 34. This causes the system
10 to store the chain number of the selected block and to alter the status
11 character of that block from "full" to "empty". The additional blocks
12 storing the selected record have the same chain number as the selected
13 block. These records are then automatically purged by the system by
14 means of altering the status character. The purging is ceased by
15 detection of an end of record symbol within the data area of one of the
16 blocks being purged.

17 A feature of the present system is that the record being
18 purged will also automatically be read out on line 31 to the CPU,
19 thereby allowing both reading and purging on a single pass of the cyclic
20 file 12.

21 Referring additionally to Fig. 4, the CPU places the system
22 in the purge mode by transmitting a command read signal on line 43
23 and a command purge signal on line 34. The signal on line 43 throws
24 switches 130-137 to the "R" position. The read circuitry therefore
25 operates identically as in the read mode, as described above.

26 The signal on line 34 operates a relay (not shown) which
27 throws switches 251 and 192 to the "P", or "Purge" position. The
28 system is now set to read data to the CPU until the CPU designates
29 the selected record by transmitting a command purge signal on line 34
30 of two character length duration. The requirement of the two

1 character length signal is a safety feature to prevent accidental purging
2 of the cyclic file.

3 The command purge line 34 is connected not only to the
4 above mentioned relay, but also to the SET OFF input to purge blocking
5 flip-flop 153. The purge blocking flip-flop comprises a conventional
6 flip-flop circuit having an integrating circuit at its SET OFF input.
7 The integrating circuit prevents the turning off of the flip-flop until
8 the input signal on command purge line 34 remains on for two character
9 times. Then, the output of the integrating circuit builds up to a suffi-
10 cient voltage to operate the flip-flop, turning it off.

11 The SET ON input to the purge blocking flip-flop is con-
12 nected to the output of detect region start circuit 142. Thus, the flip-
13 flop is reset to its normally on state at the beginning of each region by
14 the output of detect region start circuit 142. The flip-flop then remains
15 on until turned off by the special two character length command purge
16 signal which is transmitted by the CPU at the moment it recognizes the
17 data designating the record it desires to purge.

18 The function of the purge blocking flip-flop 153 is to control
19 the entire purging operation so that no purging may be accomplished
20 until the special signal is received on command purge line 34. The
21 output of the purge blocking flip-flop is connected to the control input
22 to gate 243 and to inverter 252.

23 The controlled input to gate circuit 243 is connected, via
24 switch 132 and gate circuit 241, to the output of single character
25 register 112. Gate circuit 241 is controlled by previously described
26 circuitry including chain number flip-flop 240 and four character delay
27 215 to gate therethrough only the chain number of every block having a
28 full status character. Before the two character command purge signal
29 is received, the purge blocking flip-flop is on opening the gate circuit
30 243. This allows the chain number of every full record, as transmitted

1 by gate 241 of the read circuitry, to be gated through gate 243 to purge register 155.

The purge register comprises a conventional storage register which is momentarily reset to zero by an incoming signal which then assumes the code of the number received at its input. The purge register continually applies at its output the code representative of the number stored therein. Thus, the purge register is continually updated to store the most recently received chain number until the command purge signal closes gate 243. Since a two character command purge signal is received only during the transmission to the CPU of the data from the first block of the record the CPU desires to purge, the purge register contains, after the special command purge signal, the chain number of the record to be purged.

The RESET input of purge register 155 is connected to the output of detect region start circuit 142. Thus, as the region start character is detected by circuit 143, the output therefrom on line 150 resets the purge register to zero. Therefore, the chain number cannot be stored after the first pass of the memory. This serves as another safety feature to prevent accidental purging.

20 Purge register 155 is connected to compare chain number and purge register circuit 217. This circuit is essentially identical in construction to compare block count and chain number circuit 211, previously described, except that the timing means therein leaves the output of the circuit on for the length of time equal to that required for the data area of a block to pass one head of the file. Thus, upon detecting an identical comparison between the chain number and purge register, compare circuit 217 provides a signal on its output of duration equal to the data area of a block.

25 Since the chain number for every full record is transmitted through gate 241 to one input of compare circuit 217 and also transmitted

1 via gate 243 and purge register 155 to the other gate of compare circuit 217, the circuit provides an output of one data area time immediately after the detection of the chain number of every full block until the special command purge signal is received. Upon receipt of the special command purge signal, purge blocking flip-flop 153 turns off, thereby closing gate 243 and preventing further transmission of chain numbers to purge register 155. From that time forward, the purge register 155 transmits to compare circuit 217 the chain number of the record selected by the CPU to be purged. Gate 241 continues to transmit the chain number for every full record to the other input of compare circuit 217. Therefore, circuit 217 provides an output each time the chain number of a full block is that of the record to be purged.

10 The output of purge blocking flip-flop 153 is connected, in addition to gate 243, to inverter 252. The inverter generates at its output a d.c. voltage level opposite to that of the level on its input. Therefore, when purge blocking flip-flop 153 is on, the inverter provides no signal on its output and when the purge blocking flip-flop 153 is off, the inverter provides a positive level at its output. The output of inverter 252 is connected to one input to AND circuit 253. The other 20 input to the AND circuit is connected to the output of compare circuit 217.

Since purge blocking flip-flop 153 is normally on, the output of inverter 252 is normally off thereby closing AND circuit 253 so as to block the output of compare circuit 217. Only after the special command purge signal is received on line 34 does the flip-flop 153 switch off so that the inverter provides a positive signal to one side of the AND circuit, gating the output of compare circuit 217 therethrough.

20 The CPU reads a portion of the data transmitted by the read circuitry thereto before detecting that the data being read is that of the record to be purged. Thus, the signal on line 33 is not transmitted until long after the chain number has been detected. Therefore,

1 the reason that compare circuit 217 is provided with an output of long
2 duration is so that the command purge signal will cause the output
3 therfrom to be gated by AND circuit 253 regardless of what time
4 during the reading of data from a block that the CPU transmits the
5 special command purge signal.

6 The output of AND circuit 253 is connected, via switch 251,
7 to set status empty circuit 254. The set status empty circuit is sub-
8 stantially identical to set status full circuit 200 except that its output
9 produces the code representing the status empty character. This
10 character is transmitted on cable 255 through OR circuit 203 to
11 single character register 204. The single character register stores
12 the status empty character until such time as a signal appears on
13 command readout line 205.

14 Since the CPU will provide the special command purge
15 signal toward the end of the data area of the first block of the record
16 to be purged, it is necessary to operate the timing circuitry for proper
17 gating of the status character before the command purge signal is
18 received. Therefore, the output of detect status full circuit 171 which
19 controls the timing is connected via switch 136, line 190, switch 192,
20 and OR circuit 204 directly to head delay and single shot circuit 207.

21 In this manner, the head delay is initiated upon detection
22 of every status full character so that the command readout line is
23 energized to transmit whatever is stored therein to serialiser 111 to be
24 written in the status area thereof. If during this period no command
25 purge signal is received, no output is transmitted from set status
26 empty circuit 254. Therefore, there is no data contained in the single
27 character register and nothing is transmitted therfrom as a result of
28 the command readout signal. However, if a command purge signal has
29 been received so that AND circuit 253 operates to transmit the output of
30 compare circuit 217 therethrough, set status empty circuit 254 provides

1 the status empty character to single character register 204. The
2 delayed command readout signal from head delay and single shot
3 circuit 207 then operates to cause the register to transmit the character
4 on cable 206. This character is transmitted via OR circuit 122 to
5 serialiser 111 which causes write amplifier 106 to write the status
6 empty character into the status area of the selected block. This effects
7 the purging of the block.

8 The output of inverter 252 remains on for the rest of the
9 region since purge blocking flip-flop 153 remains off thereby gating
10 subsequent outputs of compare circuit 217 therethrough. These outputs
11 indicate those blocks having a chain number of the record to be purged
12 and again allows operation of set status empty circuit 254. The status
13 empty characters are again transmitted by single character register
14 204 to be written in the status area of those blocks.

15 In the event no comparison is made by compare circuit 217,
16 nothing is transmitted through the AND gate 253 so no status empty
17 characters are written in the status areas of those blocks.

18 As the pass of the region is completed, the region start
19 character is detected by circuit 142 and the output on line 150 therefrom
20 resets purge register 155 to zero and resets purge blocking flip-flop
21 153 to its normally on state. This again opens gate 263 to allow the
22 gating of subsequent chain numbers to purge register 155 and turns off
23 inverter 252 to block AND gate 253. Therefore, no further transmis-
24 sions are allowed to set status empty circuit 254 even though switch 251
25 remains closed.

26 This is another safety factor preventing accidental purging
27 of the cyclic file.

28 PURGE OPERATION

29 Referring to Fig. 3C, the example illustrated is the purging
30 of record no. 9 from a selected region.

1 Referring additionally to Fig. 1, the program 32 of the
CPU 10 reaches an instruction commanding that a record from a selected
region of cyclic file 12 having specific identifying data be purged there-
from. To accomplish this, the CPU selects the desired region by
appropriate signals on track select line 28, which is interpreted by file
control unit 11, to select, via control line 29, the desired track. The
CPU then transmits a signal on command read line 43 and a signal on
command purge line 34.

10 Referring additionally to Fig. 4, the signal on line 43
operates a switching means to throw switches 130-137 to the "R"
position so that the system assumes the read mode. The signal on
line 34 operates another switching means (not shown) to throw switches
251 and 192 to the "P" or "Purge" position. This sets the system to
the purge mode in addition to the read mode.

The operation of the read portion of the system is identi-
cal to that described with respect to the read operation described above.
Therefore, the operation of the read circuitry will not be described
except in cursory fashion.

20 After the switches have been thrown, nothing of importance
happens until the region start character is read by read head 101 and
read amplifier 105 and deserialized by deserializer 110. Upon comple-
tion of the deserialization, at the end of the character time, the
parallel data is transmitted to single character register 112. The
register stores the data for one character time during which it trans-
mits the data on cable 140. The region start character on cable 140 is
detected by region circuit 142 which transmits a signal on line 150.

This signal resets the read circuitry and also resets purge
register 155 to zero and is received at the SET ON input to purge block-
ing flip-flop 153. This turns on the flip-flop if it was not already on.
The output of the flip-flop is applied to the control input to gate 243

1 turning the gate on so that it transmits data received at the controlled inputs therethrough. The output of the flip-flop is also applied to inverter 252 which inverts the signal and thereby turns off AND circuit 253 preventing the transmission of signals therethrough.

The first block to be detected is block no. 1, which has record no. 9 stored therein. Record no. 9 is the block to be purged. The block start character for block no. 1 is detected by detect block start circuit 143 and the output therefore operates the various read circuitry and is counted by block counter 151. The status character of 10 block no. 1 is detected by detect status full circuit 171 since the block is full and an output transmitted on line 190. This output is transmitted via switch 192 and OR circuit 201 to begin operation of head delay and single shot circuit 207. The status character also operates various read circuitry to gate the chain number immediately following through gate circuit 241. Therefore, the chain number, which is the number "1", is gated through gate 241 to one input of compare chain number and purge register 217 and to the control input of gate circuit 243. As previously explained, gate circuit 243 is open so that the data is transmitted to purge register 155. The purge register stores the data therein and transmits the number to the other input of compare circuit 217.

20 Since the chain number and the output of the purge register 155 are identical, compare circuit 217 then provides an output signal equal to the data area of block no. 1 to one input of AND circuit 253. However, the AND circuit remains off blocking the transmission of the signals therethrough.

Then, the read circuitry causes the transmission of the data from the data area of block no. 1 to the CPU on cable 31. The program 32 of the CPU subsequently detects that the data being read is that designating the record to be purged. Therefore, the CPU does 30 not transmit a reject signal on line 33 and does transmit a special two-

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1 character purge signal on line 34.

2 The special command purge signal is detected by the integrat-
3 ing circuit at the SET OFF input of purge blocking flip-flop 153,
4 turning the flip-flop off. This closes gate 243 and causes inverter 252
5 to provide a positive output. This output operates AND circuit 253 to
6 gate the output of compare circuit 217 therethrough. This output is
7 transmitted, via switch 251, to set status empty circuit 254.

8 The set status empty circuit then responds by transmitting
9 the status empty character via line 255 and OR circuit 203 to single
10 character register 204. The single character register then stores the
11 status empty character.

12 As the status character position of record no. 1 comes
13 adjacent to write head 102, head delay and single shot circuit 207 pro-
14 vides a signal on command readout line 205 commanding the single
15 character register to transmit the status empty character onto cable
16 206. The status empty character is then serialised by serialiser 111
17 and written by write amplifier 105 and write head 102 into the status
18 character position of block no. 1.

19 Therefore, the status full character of block no. 1 has
20 operated head delay and single shot 207, the chain number of block no. 1
21 has been stored in purge register 153, and the data therefrom trans-
22 mitted to the CPU. The CPU has indicated that that data designates the
23 record to be purged and responded by transmitting a special command
24 purge signal on line 34. This signal has gated the output of compare
25 circuit 217 to set the status empty character into the status position of
26 the record as controlled by the timing of head delay and single shot 207.

27 Block no. 2 is then detected by read head 101. The block
28 start character thereof causes operation of the status circuitry to gate
29 the subsequent status character to circuits 171 and 172. Detect status
30 full circuit 171 provides an output on line 190 which initiates operation

1 of head delay and single shot 207. The output also operates one character
2 delay 191 to subsequently operate the chain number circuitry to gate the
3 chain number to gate 243 and to one input of compare chain number and
4 purge register 217.

5 Purge blocking flip-flop 153 is off due to the special command
6 purge signal received during the previous block. Therefore, gate 243
7 blocks the transmission of the chain number to purge register 155. The
8 output of purge register 155 to the other input of compare circuit 217 is
9 therefore the previous chain number, number "1".

10 The chain number of block no. 2, however, is also the
11 number "1". Therefore, the compare circuit provides an output to
12 AND circuit 253 of duration equivalent to that of one data area.

13 Also as a result of purge blocking flip-flop 153 being off,
14 inverter 252 provides a positive signal to the other input of AND circuit
15 253. Therefore, the output of compare circuit 217 is gated therethrough
16 to thereby operate set status empty circuit 254. Circuit 254 then trans-
17 mits the status empty character to single character register 204 which
18 stores the character until the status area of record no. 2 is adjacent
19 write head 102 at which time head delay and single shot circuit 207
20 provides a signal on command readout line 205 causing the register to
21 transmit the status empty character to serializer 111. Serializer 111
22 then provides a serial translation of the character to write amplifier 106,
23 which causes the character to be written into record no. 2.

24 Thus, since a chain number of record no. 2 was the same
25 as that stored in purge register 155, the output of compare circuit 217
26 causes the status empty character to be written into the status position
27 of the record as controlled by the timing of head delay and single shot 207.

28 Likewise, record no. 3 also contains as its chain number,
29 the number "1". Therefore, compare circuit 217 again provides an
30 output which is gated to set status empty circuit 254. Again, circuit 254

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1 causes the status empty character to be written into the status position
2 of record no. 2, as controlled by the timing of head delay and single
3 shot 207.

4 Block no. 4 is also full and the resultant output of detect
5 status full circuit 171 gates the chain number thereof to compare cir-
6 cuit 211 for comparison with the output of purge register 155. Here,
7 the chain number is the number "4" while the output of purge register
8 155 is the number "1". Thus, compare circuit 217 does not provide an
9 output and the command readout signal from head delay and single shot
10 207 operates single character register 204, but gates nothing therefrom
11 since set status empty circuit 254 was not actuated.

12 Likewise, blocks 5-23 are all indicated as being full, but
13 the chain number does not agree with the chain number "1" of record
14 no. 9. Therefore, no status empty characters are transmitted.

15 The status full character from block no. 24 operates head
16 delay and single shot 207 and operates the chain number circuitry to
17 gate the chain number thereof to compare circuit 217. As shown, the
18 chain number of block no. 24 is the number "1", which agrees with the
19 output of the purge register. Therefore, the compare circuit transmits
20 an output through AND circuit 253 to operate set status empty circuit
21 254. The resultant status empty character is transmitted by single
22 character register 204 and the time controlled by head delay and single
23 shot 207 to serialiser 111. The character is then serialised and written
24 into the status area of block no. 24.

25 At some point during the reading of data from block no. 24,
26 an end of record character is transmitted through gate 141 onto cable
27 244. The character is detected by detect end of record circuit 231 and
28 an output provided on line 182. This output turns off the block length
29 circuitry to terminate the transmission of data to the CPU.

30 As shown, all subsequent blocks in the region are indicated

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1 as being empty. Therefore, detect status full circuit 171 provides no
2 output onto line 190 and the outputs of detect status empty circuit 172
3 are prevented by AND circuit 198 and switch 136 from transmitting a
4 signal onto line 190. Therefore, no further chain numbers are gated
5 to compare circuit 217 and no further purge outputs are provided
6 therefrom.

7 Upon the completion of the complete scan of the region, the
8 region start character is detected by circuit 142 and the resultant output
9 on line 190 resets purge blocking flip-flop 153 to its normal on state.
10 Additionally, the output resets purge register 155 to zero. The turning
11 on of purge blocking flip-flop 153 turns off inverter 252 to block any
12 outputs from compare circuit 217 thereby preventing further purge
13 signals therefrom until such time as a special command purge signal
14 is received on line 34 from the CPU.

15 Therefore, the described system has read to the CPU the
16 data of block no. 1, the CPU detected that the data was that of the block
17 to be purged and thereby supplied the special purge signal to file control
18 unit 11. This signal caused the system to change the status character
19 in block no. 1 from "full" to "empty", and to store the chain number "1"
20 of the record no. 9 in purge register 155. The system then similarly
21 changed the status character of all blocks having the chain number "1"
22 from "full" to "empty" and skipped all those records not having the
23 chain number "1" of record no. 9. Finally, the end of record character
24 in block no. 24 ended the transmission of data to the CPU and the sub-
25 sequently detected region start character reset the system.

26 ADDITIONAL SYSTEMS

27 The arrangement of the system described above is dependent
28 not only on the above described method, but also upon the specific format
29 used for the blocks. Thus, the system has been shown designed in a
30 certain way to utilize the control characters designating the region start

1 and block start and to utilize the strict format that the chain number
2 always comprises four characters and that the data area of a block
3 always comprises the same number of characters designated by block
4 length counter 224. The system is also dependent upon the fact that the
5 block itself is always organized as shown in Fig 2 in that the status
6 character 23 always follows the start character 22, the chain number 24
7 always follows the status character, and the data area 25 always follows
8 the chain number.

9 Therefore, by changing the format for the blocks of data,
10 and/or by deleting or adding other control characters, the system for
11 accomplishing the described method must accordingly be altered.

12 One example of such a change is the addition of the control
13 character, "chain number follows". The use of such a character allows
14 the placing of the chain number for the first block of each record at the
15 end of the block, immediately preceded by the character "chain number
16 follows".

17 Such a character has the advantage of allowing the CPU to
18 read all of the data in the data area of a block and then to utilize the
19 chain number time to decide whether the desired record was being
20 detected. Subsequent blocks containing the same record would then
21 have the chain number located immediately after the status character,
22 as described in the above system.

23 The system then must be changed to operate on the chain
24 number as a result of detecting the chain number follows character
25 rather than depending upon the chain number immediately following
26 the status character, as above.

27 Another example of such a change is the addition of the
28 control character "data follows". This character keys the system to
29 expect data immediately thereafter rather than to depend upon delay
30 or clocking circuits to gate the output of the reading means a predeter-

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1 mixed time after the beginning of a block.
2 If the data follows a chain number, it allows the use of
3 chain numbers of variable length since it automatically signals the
4 end of the chain number and the beginning of data.

5 While the invention has been particularly shown and
6 described with respect to preferred embodiments thereof, it will
7 be understood by those skilled in the art that various changes in
8 form and details may be made therein without departing from the
9 spirit and scope of the invention.

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STK V. EMC
STK 28151

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The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A method of organizing a cyclical file comprising the steps of:
 - 3 dividing said cyclical file into a plurality of regions;
 - 4 further dividing each of said regions into a plurality of blocks;
 - 6 initially storing records sequentially beginning in the first block of a desired one of said regions;
 - 8 purging selected records from said region of said cyclical file by effectively erasing each one of said blocks wherein a record to be purged is located; and
 - 11 storing additional records in said region of said cyclical file beginning in the first available block in said region and sequentially thereafter in subsequent available blocks of said region as needed,
 - 14 whereby the stored data is packed toward the front of said region.

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STK V. EMC
STK 28152

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1 2. A method of organising a cyclical file comprising the
2 steps of:
3 dividing said cyclical file into a plurality of regions;
4 further dividing each of said regions into a plurality of
5 blocks;
6 initially storing records sequentially beginning in the first
7 block of a desired one of said regions;
8 designating each block storing a common record by
9 recording a common chain character therein, each common chain
10 character being different for each record;
11 purging selected records from said region of said cyclical
12 file by effectively erasing each one of said blocks wherein a record to
13 be purged is located, as designated by said common chain character
14 recorded therein;
15 storing additional records in said region of said cyclical
16 file beginning in the first available block in said region and sequentially
17 thereafter in subsequent available blocks of said region as needed,
18 whereby the stored data is packed toward the front of said region; and
19 designating each block storing a common one of said
20 additional records by recording a common chain character therein,
21 whereby all of the blocks storing a common record are designated by
22 a common chain character.

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STK V. EMC
STK 28153

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1 3. The method of claim 2 wherein said purging step
2 includes the steps of:
3 reading data from each record stored in said region of
4 said cyclical file as said records are detected until data from a
5 selected record is detected;
6 detecting the chain character of the block from which said
7 data was read; and
8 purging said selected record from said region by effectively
9 erasing each of said blocks wherein said detected chain character is
10 located.

1 4. The method of claim 3 wherein:
2 said reading step comprises reading data from the first
3 block of each record stored in said region as encountered until data
4 from a selected record is detected.

1 5. The method of claim 4 wherein:
2 said first block of each record is designated by being the
3 first block having a chain character not previously detected during
4 the present pass of said region.

1 6. The method of claim 2 wherein:
2 each said common chain character designating a particular
3 record comprises the sequential number within said region of the block
4 wherein the first portion of data from said record is stored.

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STK V. EMC
STK 28154

7. The method of claim 2, 3 or 4 wherein:
each said chain character designating a particular record comprises
the sequential number within said region of the block wherein the first por-
tion of data from said record is stored, whereby, in said reading step,
said first block of each record stored in said region is indicated by its
having a chain number identical to the sequential number of the block
within said region.

8. The method of claim 1, 2 or 6 wherein:
said initial storing and said storing of additional records additionally
includes the recording of a special character within each one of said
blocks in which said records are stored, said special character indicating
that said blocks are full;
said effective erasure comprises the erasure of said special
character within each one of said blocks so erased; and
said available blocks being detected by detecting the absence of said
special character within a block.

9. The method of claim 1 wherein:
said step of dividing each of said regions into a plurality of blocks
additionally includes the step of recording of a special character which
indicates that the block is empty;
said initial storing of records additionally includes the erasure of said
special character in those blocks in which data is stored;
said effective erasure of each one of said blocks to be purged
comprises the recording of said special character in each of said blocks;
the detection of said available blocks comprises the detection of said
special character therein; and
said recording of additional records comprises additionally the erasure
of said special character appearing in those blocks in which said additional
records are recorded.

1 10. A method of organising a cyclical file comprising the
2 steps of:
3 dividing said cyclical file into a plurality of regions;
4 further dividing each of said regions into a plurality of
5 blocks;
6 writing a first special character in each one of said blocks
7 to indicate that said blocks are empty;
8 initially storing records sequentially beginning in the first
9 block of a desired one of said regions;
10 erasing said first special character in each one of said
11 blocks in which said records are stored;
12 recording a second special character in each of said blocks
13 in which said records are stored to indicate that said blocks are full;
14 purging selected records from said region of said cyclical
15 file by erasing said second special character and recording said first
16 special character in each one of said blocks wherein a record to be
17 purged is located;
18 storing additional records in said region of said cyclical
19 file beginning in the first available block in said region by detecting
20 the first block in said region having said first special character therein
21 and sequentially thereafter in subsequent available blocks of said region
22 as needed, said available blocks being detected by the detection of said
23 first special character therein; and
24 erasing said first special character and recording said
25 second special character in each of said blocks wherein said additional
26 records are stored.

1 11. The method of claim 1 further including the step of:
2 reading selected records from said cyclical file.

12. The method of claim 11 wherein said reading step includes the steps of:

reading data from each record stored in said region of the file until data designating a selected record is detected; and

subsequently reading all subsequent blocks containing data of the same record.

13. A data storage system for storing data records comprising:
a cyclical data storage means divided into a plurality of regions of selected lengths, each region being divided into a plurality of blocks;
reading means for reading stored data in said data storage means;
writing means for subsequently storing data in said data storage means;
detection means responsive to said reading means for detecting whether a block is empty; and
gating means responsive to the output of said detection means for gating data to said writing means for the duration of said empty block.

14. A data storage system for storing data records, each said record terminating with a special character, comprising:

a cyclical data storage means divided into a plurality of regions of selected lengths, each region being divided into a plurality of blocks;
reading means for reading stored data in said data storage means;
writing means for subsequently storing data in said data storage means;
region detection means for detecting the beginning of a selected region;
status detection means responsive to said reading means for detecting whether a block is empty; and
gating means responsive to said region detection means, said status detection means, and said special character for gating a data record to said writing means for the duration of the first said detected empty block subsequent to said detection of the beginning of said selected region, and

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for the duration of each following detected empty block until terminated by the gating of said special character.

15. The apparatus of claim 13 or 14 for storing data records further including:

means for designating the ones of said blocks containing each particular one of said data records.

16. The apparatus of claim 13 or 14 further including:

purging means for effectively emptying selected ones of said blocks.

1 17. A data storage system for storing data records
2 comprising:
3 a cyclical data storage medium divided into a plurality of
4 regions of selected lengths, each region being divided into a plurality
5 of blocks of equal length;
6 reading means mounted for reading recorded data on said
7 data storage medium;
8 writing means mounted behind said reading means for
9 subsequently recording data on said data storage medium;
10 region detection means for detecting the start of a selected
11 region and resetting and rendering said system effective upon making
12 such detection;
13 gateable buffer means for temporarily storing said data
14 records to be written, the output thereof being connected to said
15 writing means;
16 block detection means responsive to said reading means
17 for detecting whether a block is empty;
18 block indication means responsive to the operation of said
19 block detection means for storing a chain character representative of
20 the first detected empty block and for operating said writing means to
21 write said chain character at the beginning of said first and each
22 subsequently detected empty block;
23 gate operation means responsive to the operation of said
24 block detection means for gating said gateable buffer means at a
25 specified time and for a specified duration to thereby supply said data
26 to said writing means between said chain character and the end of said
27 block; and
28 termination means for detecting the end of said data record
29 being written to terminate the operation of said block indication means
30 and said gate operation means.

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1 18. The apparatus of claim 17 further including purging
2 means comprising:
3 purge selection means responsive to said reading means
4 for detecting a selected record to be purged;
5 chain detection means responsive to said purge selection
6 means and said reading means for detecting and storing the chain
7 character of the block from which said selected record was detected; and
8 erasing means responsive to said chain detection means
9 for effectively erasing each of said blocks wherein said stored chain
10 character is detected.

1 19. The apparatus of claim 18 wherein said purging
2 means further includes:
3 selection gating means responsive to said reading means
4 for reading the chain character of each full block and gating the
5 output of said reading means to said purge selection means upon
6 detecting a chain character not previously detected during the
7 present pass of said region.

1 20. The apparatus of claim 19 wherein:
2 said block indication means comprises counting means
3 responsive to said reading means for counting each block detected
4 after the start of said region, means for storing as said chain
5 character the count present in said counter upon the operation of said
6 detection means, and means for operating said writing means to write
7 said character at the beginning of the first and each subsequently
8 detected empty block; and
9 said selection gauging means responds to said reading
10 means and said counting means of said block indication means to
11 gate each one of said blocks having a chain number identical to said
12 count until said purge selection means is operated.

21. The apparatus of claim 18 or 19 wherein:

 said block indication means additionally includes means for operating said writing means to write a special status character indicating that a block is full immediately preceding said chain character at the beginning of said first and each subsequently detected empty block;

 said erasing means comprises means for erasing said status character in each of said blocks wherein said stored chain character is detected; and

 said block detection means comprises means for detecting the absence of said status character within a block.

22. The apparatus of claim 18 or 19 wherein:

 each of said blocks of said region additionally includes an initially recorded special status character at the beginning thereof indicating that the block is empty;

 said block detection means comprises means for detecting said status character at the beginning of a block, thereby detecting whether such block is empty;

 said block indication means additionally includes means responsive to the operation of said block detection means for erasing said status character from said first and each subsequently detected empty block; and

 said erasing means of said purging means comprises means for writing said status character at the beginning of each of said blocks wherein said chain character is detected.

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1 23. A data storage system for storing data records
2 comprising:
3 a cyclical data storage medium divided into a plurality of
4 regions of selected lengths, each region being divided into a plurality
5 of blocks of equal length, each block having an initially recorded first
6 status character at the beginning thereof indicating that said block is
7 empty;
8 reading means mounted for reading recorded data on said
9 data storage medium;
10 writing means mounted behind said reading means for
11 subsequently recording data on said data storage medium;
12 region detection means for detecting the start of a selected
13 region and resetting and rendering said system effective upon making
14 such detection;
15 gateable buffer means for temporarily storing said data
16 records to be written, the output thereof being connected to said
17 writing means;
18 block detection means for detecting said first status charac-
19 ter at the beginning of a block, thereby detecting whether such block is
20 empty;
21 block indication means responsive to the operation of said
22 block detection means for erasing said first status character at the
23 beginning of said first and each subsequently detected empty block and
24 recording thereof a second status character indicating that each said
25 block is full, for storing a chain character representative of the first
26 detected empty block, and for operating said writing means to write
27 said chain character immediately after said second status character
28 in said first and each subsequently detected empty block;
29 gate operation means responsive to the operation of said
30 block detection means for gating said gateable buffer means at a

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Claim 23 - Cont'd.

31 specified time and for a specified duration to thereby supply said data
32 to said writing means between said chain character and the end of said
33 block;
34 purge selection means responsive to said reading means
35 for detecting a selected record to be purged;
36 chain detection means responsive to said purge selection
37 means and said reading means for detecting and storing the chain
38 character of the block from which said selected record was detected;
39 erasing means responsive to said chain detection means
40 for erasing said second status character in each of said blocks wherein
41 said stored chain character is detected and for writing said first status
42 character therefor in each of said blocks; and
43 termination means for detecting the end of said data record
44 being written to terminate the operation of said block indication means
45 and said gate operation means.

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24. The data storage system of claim 18 further including
read selection means responsive to said reading means for detecting
a selected record to be read;
chain detection means responsive to said read selection means and
said reading means for detecting and storing the chain character of the block
from which said selected record was detected; and
transmission means responsive to said last mentioned chain detec-
tion means for transmitting data from each of said blocks wherein said stor-
ed chain character is detected.

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1 25. A data storage system for storing data records
2 comprising:
3 a cyclical data storage medium divided into a plurality of
4 regions of selected lengths, the beginning of each region being denoted
5 by a special region start character, and each region being divided
6 into a plurality of blocks, the beginning of each block being denoted by
7 a special block start character;
8 reading means mounted for reading recorded data on said
9 data storage medium;
10 writing means mounted behind said reading means for
11 subsequently recording data on said data storage medium;
12 region detection means for detecting said region start
13 character and resetting and rendering said system effective upon
14 making such detection;
15 gateable buffer means for temporarily storing said data
16 records to be written, the output thereof being connected to said
17 writing means;
18 block detection means responsive to said reading means
19 and activated by each said block start character for detecting whether
20 each block is empty;
21 block indication means responsive to the operation of said
22 block detection means for storing a chain character representative of
23 the first detected empty block and for operating said writing means to
24 write a special keying character immediately followed by said chain
25 character in the first and each subsequently detected empty block;
26 gate operation means responsive to the operation of said
27 block detection means for causing said gateable buffer means to thereby
28 supply said stored data to said writing means for writing said stored
29 data in said first and each subsequently detected empty block, and
30 termination means for detecting the end of said data record
31 being written to terminate the operation of said block indication means
32 and said gate operation means.

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1 26. The apparatus of claim 25 further including purging
2 means comprising:
3 purge selection means responsive to said reading means
4 for detecting a selected record to be purged;
5 chain detection means responsive to said purge selection
6 means and said reading means and operated by said keying character
7 for detecting and storing the chain character of the block from which
8 said selected record was detected; and
9 erasing means responsive to said chain detection means
10 for effectively erasing each of said blocks wherein said stored chain
11 character is detected.

1 27. The apparatus of claim 26 wherein said purging
2 means further includes:
3 selection gating means responsive to said reading means
4 and operated by said keying character for reading the chain character
5 of each full block and gating the output of said reading means to said
6 purge selection means upon detecting a chain character not detected
7 during the present pass of said rotation.

28. The apparatus of claim 27 wherein:

said block indication means comprises counting means responsive to said reading means for counting each block start character detected after detection of said region start character, means for storing as said chain character the count present in said counter upon the operation of said detection means, and means for operating said writing means to write said keying character immediately followed by said chain character in the first and each subsequently detected empty block; and

said selection gating means is responsive to said reading means and said counting means of said block indication means to gate each one of said blocks having a chain number identical to said count until said purge selection means is operated.

29. The apparatus of claim 26, 27 or 28 wherein:

said block indication means additionally includes means for operating said writing means to write a special status character indicating that a block is full immediately following said block start character of said first and each subsequently detected empty block;

said erasing means comprises means for erasing said status character in each of said blocks wherein said stored chain character is detected; and

said block detection means comprises means for detecting the absence of said status character within a block.

30. The apparatus of claim 26, 27 or 28 wherein:

each of said blocks of said region additionally includes an initially recorded special status character immediately following said block start character indicating that the block is empty;

said block detection means comprises means operated by said block start character for detecting said status character, thereby detecting whether such block is empty;

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said block indication means additionally includes means responsive to the operation of said block detection means for erasing said status character from the first and each subsequently detected empty block; and said erasing means of said purging means comprises means operated by said block start character for writing said status character immediately following said block start character of each of said blocks wherein said character is detected.

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Claim 31 -Cont'd.

31 empty block;

32 gate operation means responsive to the operation of said

33 block detection means for gating said gateable buffer means to thereby

34 supply said stored data to said writing means for writing said stored

35 data in said first and each subsequently detected empty block;

36 purge selection means responsive to said reading means

37 for detecting a selected record to be purged;

38 chain detection means responsive to said purge selection

39 means and said reading means and operated by said keying character

40 for detecting and storing the chain character of the block from which

41 the said selected record was detected;

42 erasing means responsive to said chain detection means

43 and operated by said block start character for erasing said second

44 status character in each of said blocks wherein said stored chain

45 character is detected and for writing said first status character

46 therefore in each of said blocks; and

47 termination means for detecting the end of said data

48 record being written to terminate the operation of said block indication

49 means and said gate operation means.

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32. The data storage system of claim 25, 26 or 27 further including:

read selection means responsive to said reading means for detecting a selected record to be read;

chain detection means responsive to said read selection means and said reading means and operated by said keying character for detecting and storing the chain character of the block from which said selected record was detected; and

transmission means responsive to said chain detection means for transmitting the data from each of said blocks wherein said stored chain character is detected.

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PATENT AGENT FOR THE
APPLICANT

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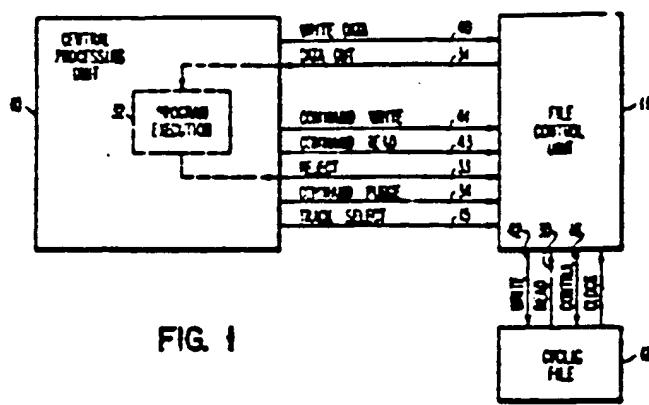


FIG. 1

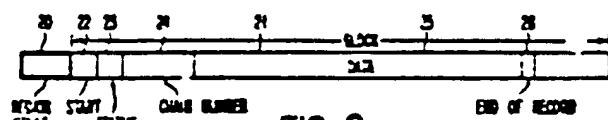


FIG. 2

FIG 3A

FIG. 3B

FIG. 3C

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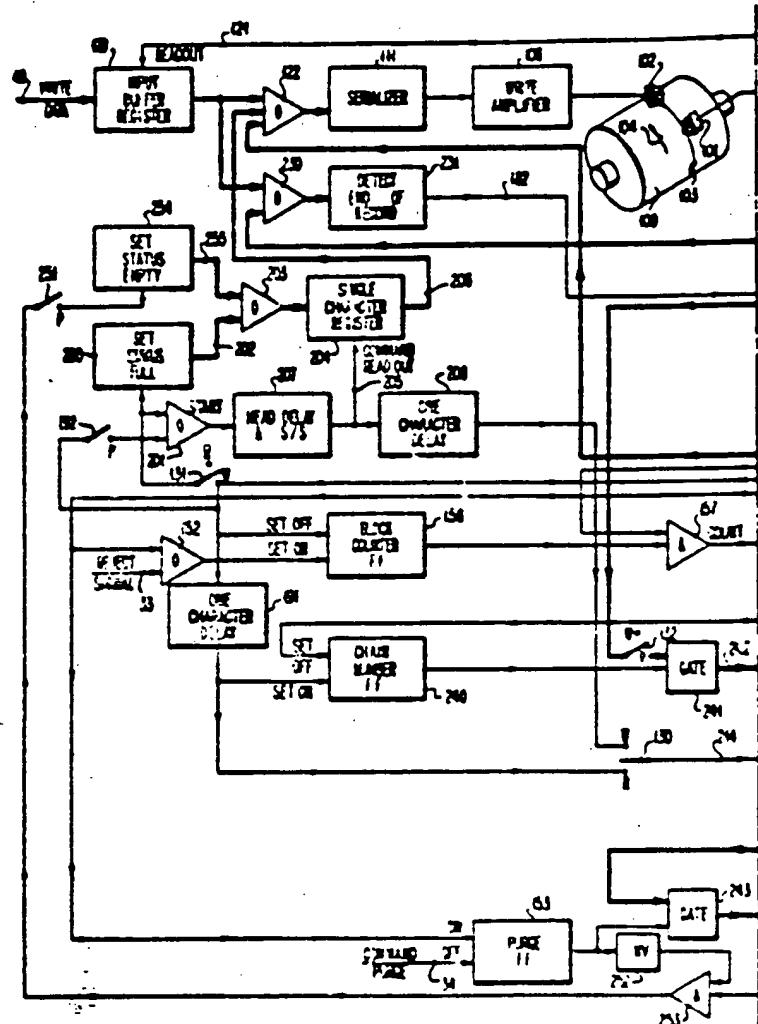


FIG. 4A

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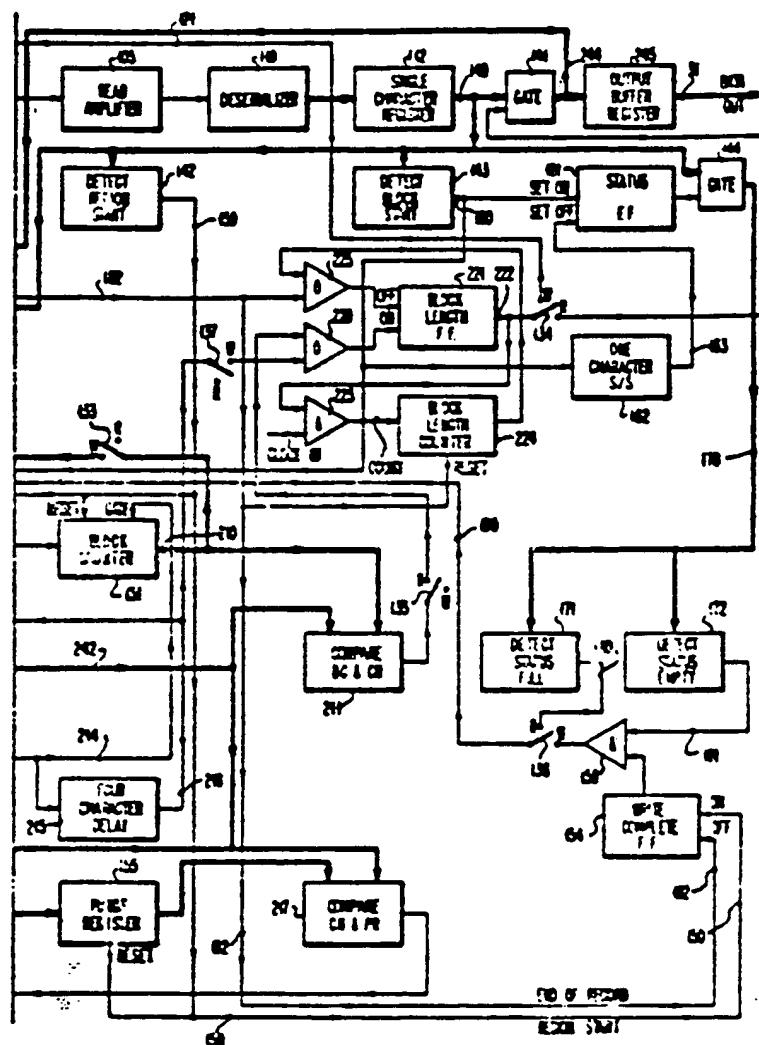


FIG. 4B

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